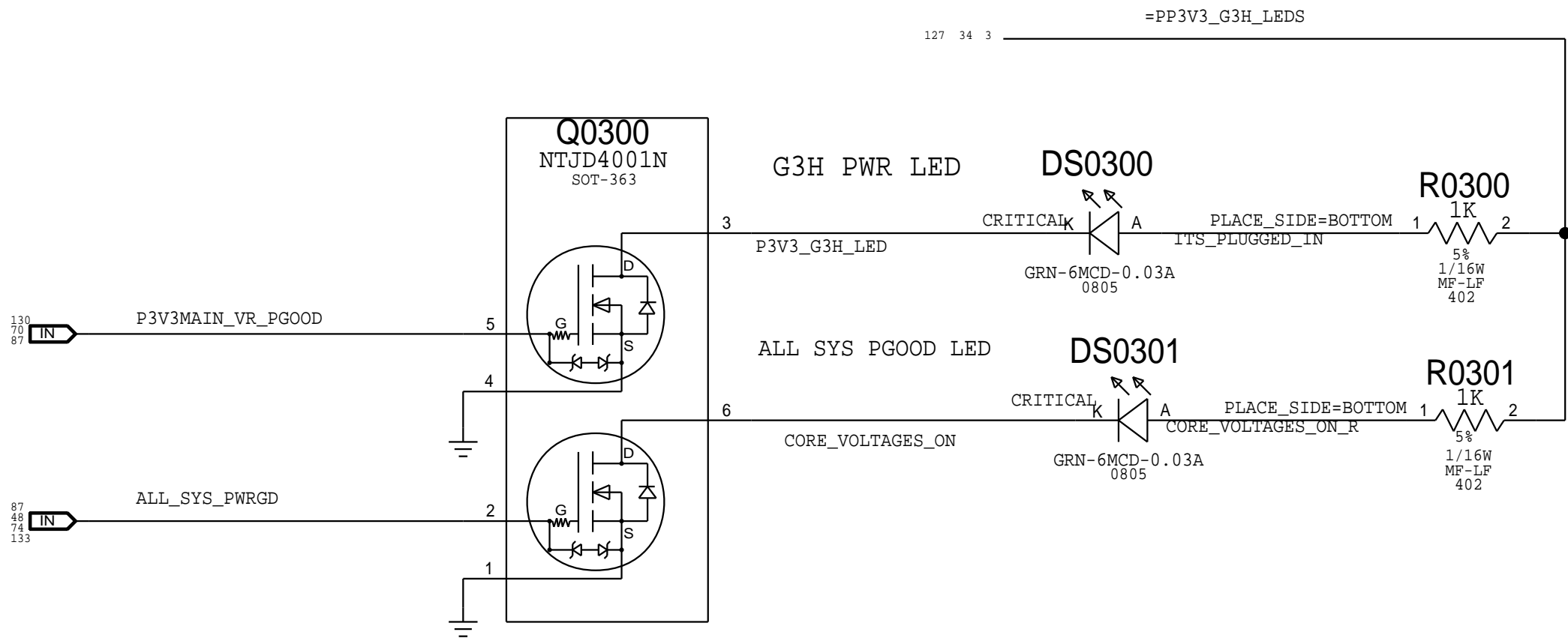
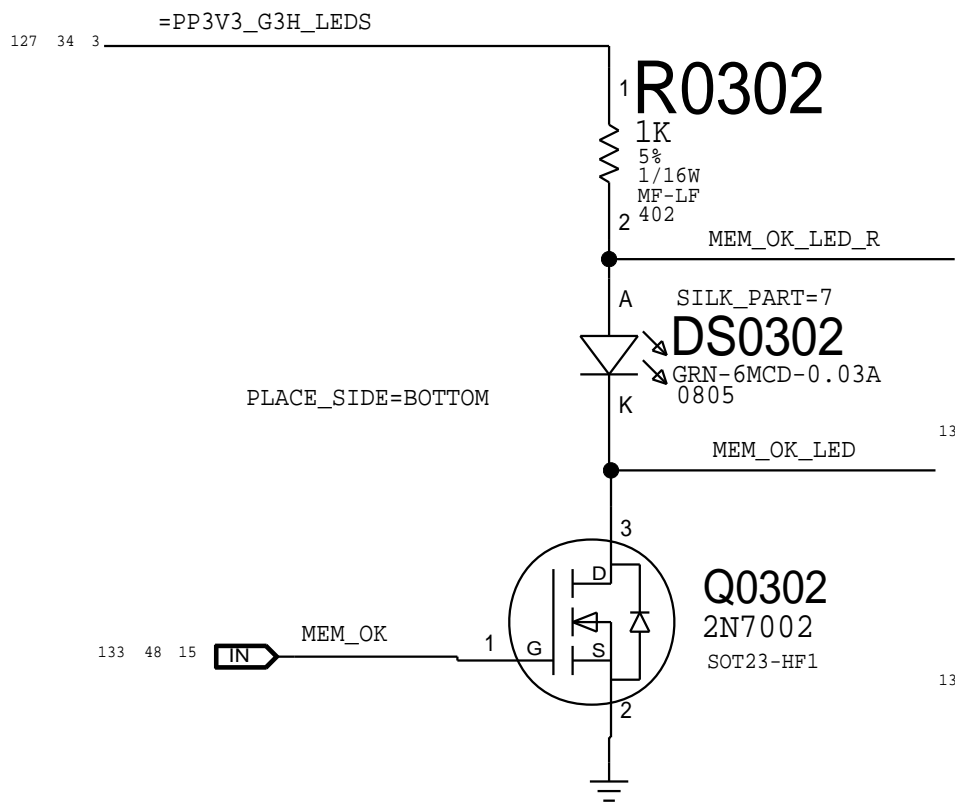


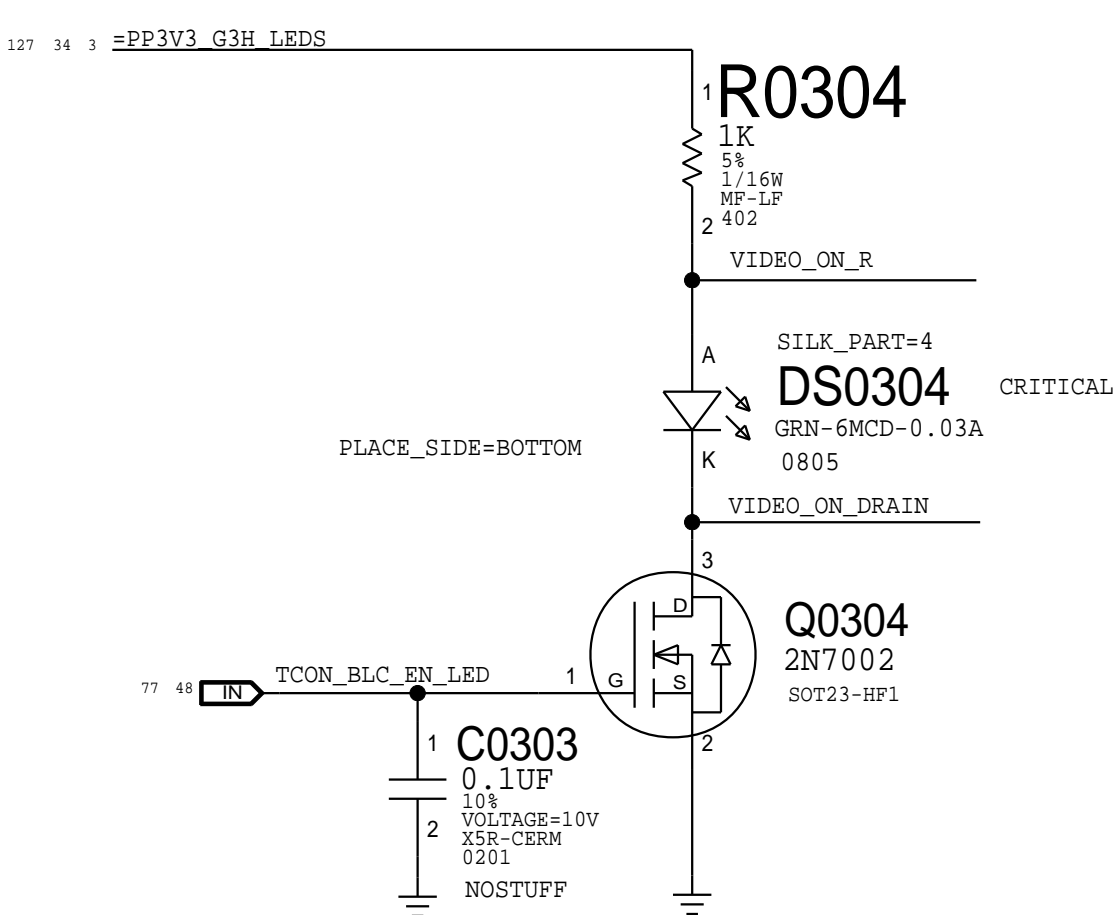
POR LEDS



MEM_OK LED

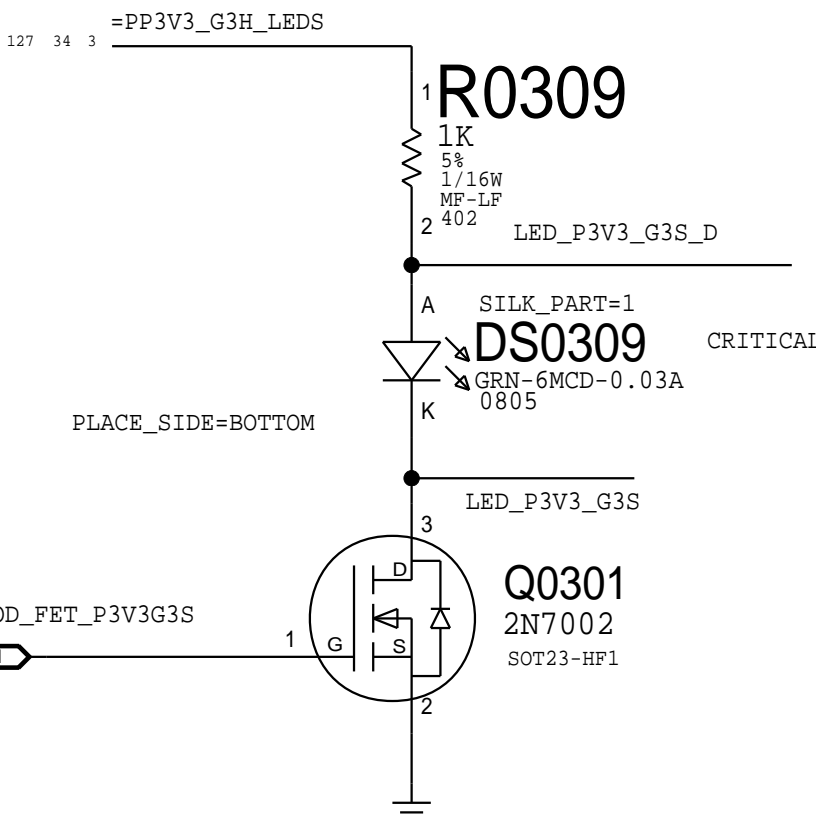
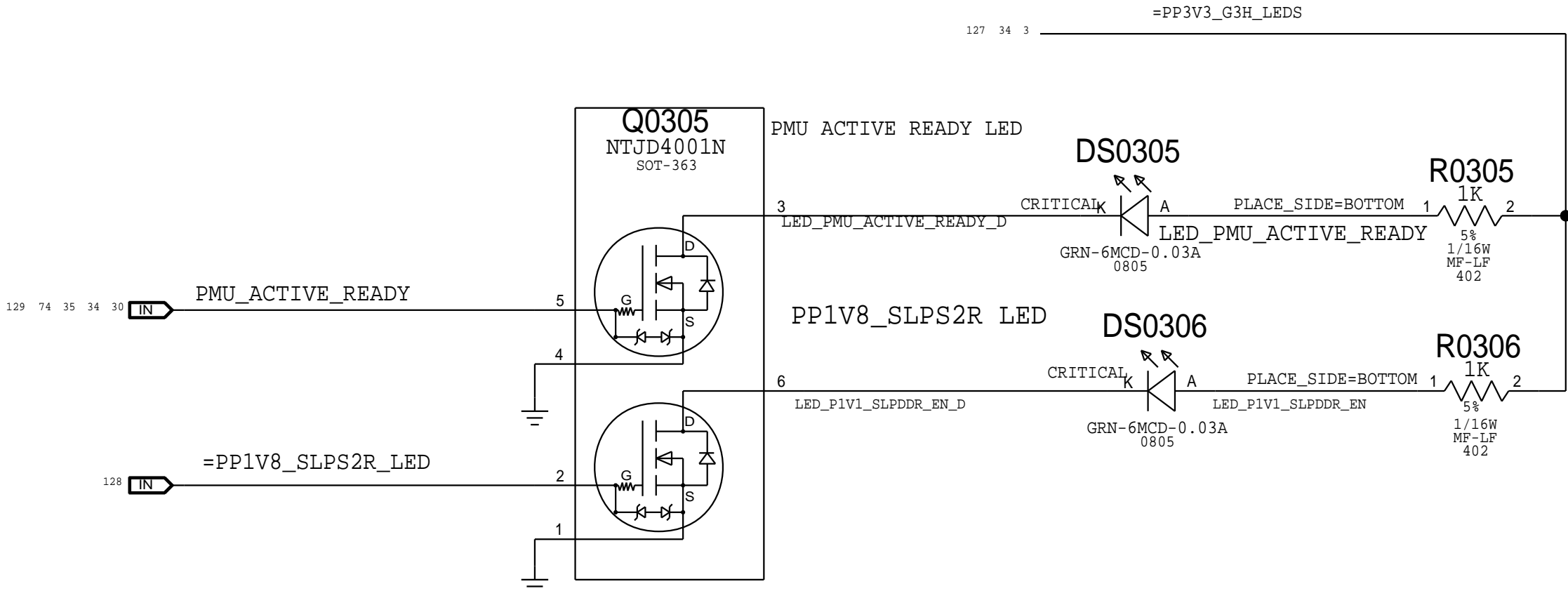


TCON OK LED



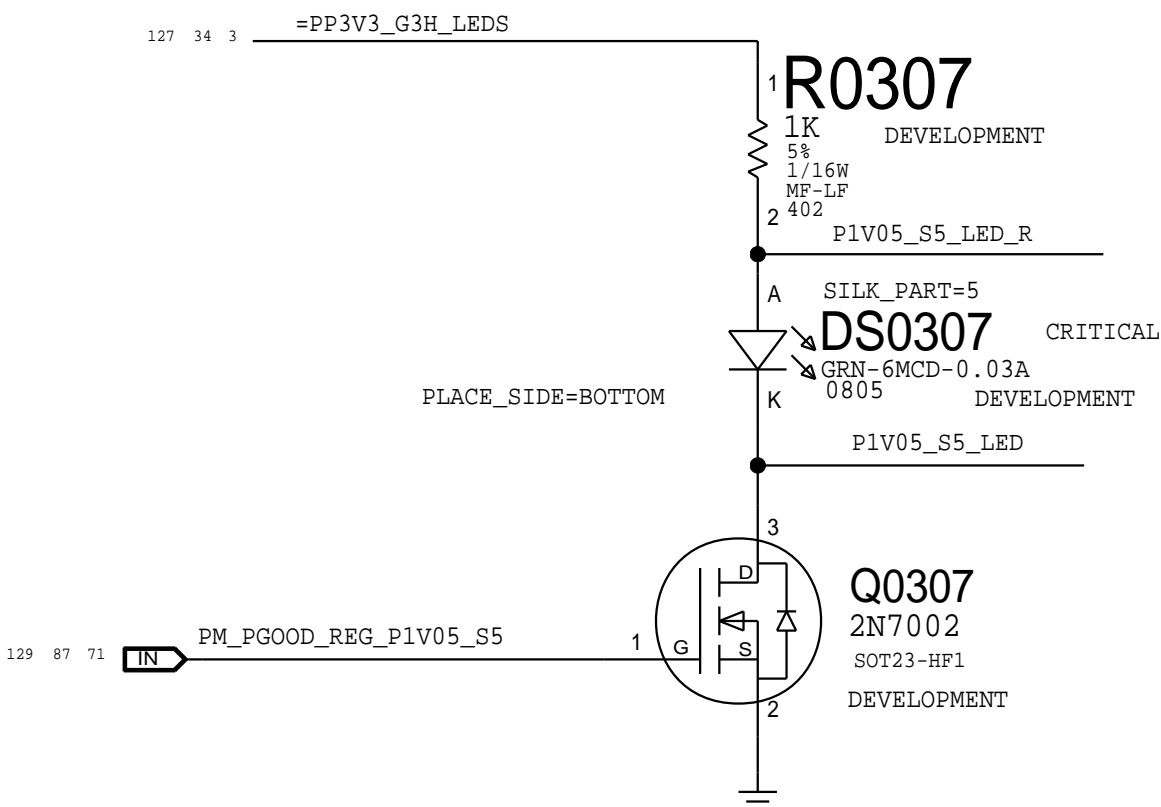
THIS LED IS DRIVEN BY GPU:
GFX_OK HIGH LIGHTS THE LED DIMLY
DP_LINK_OK HIGH LIGHTS THE LED FULLY

PP3V3 G3S LED

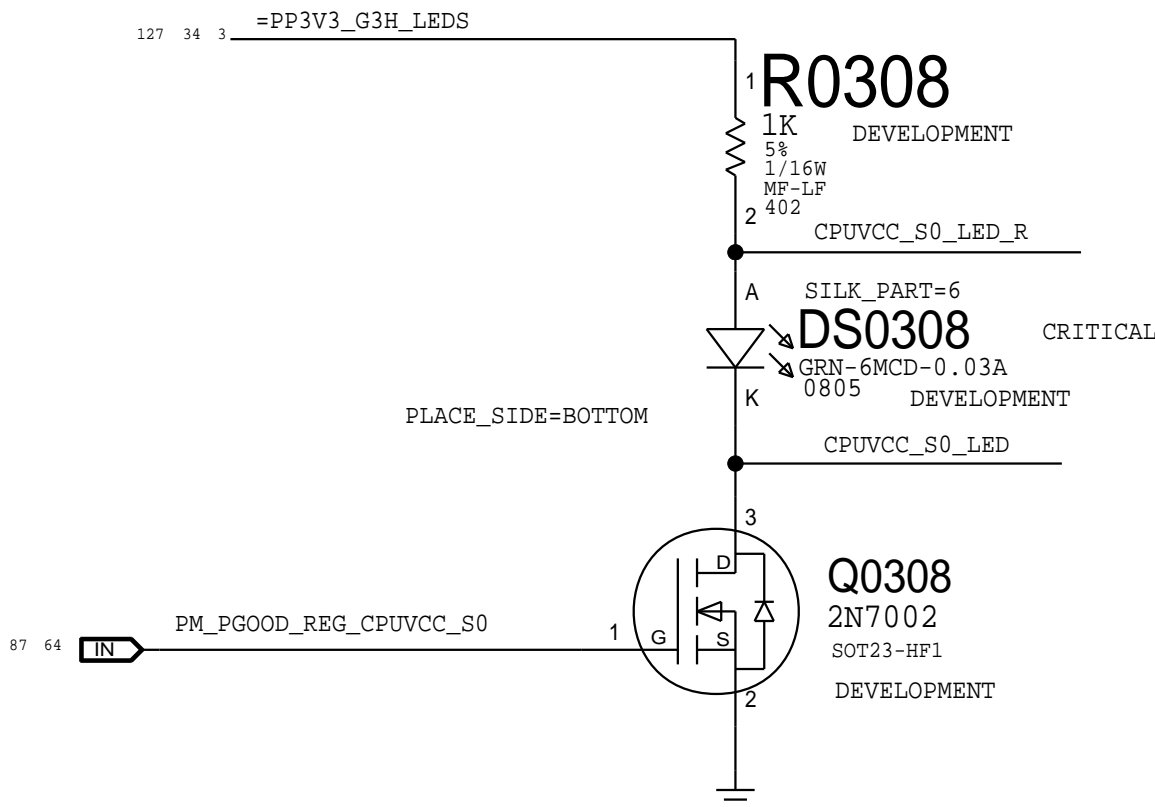


DEBUG LEDS (DEVELOPMENT ONLY)

P1V05_S5_PWRGD LED

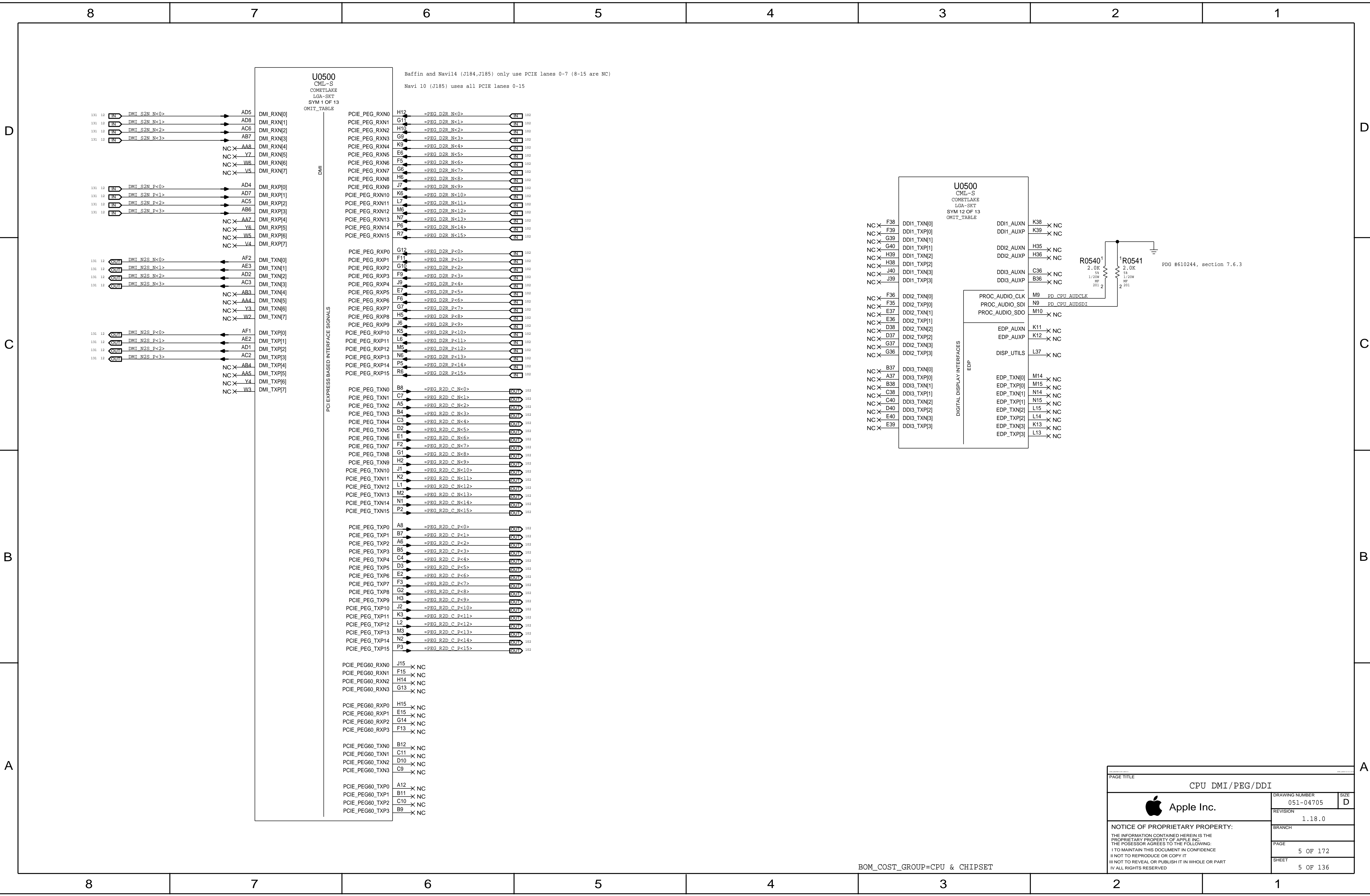



CPUVCC_S0_PWRGD LED



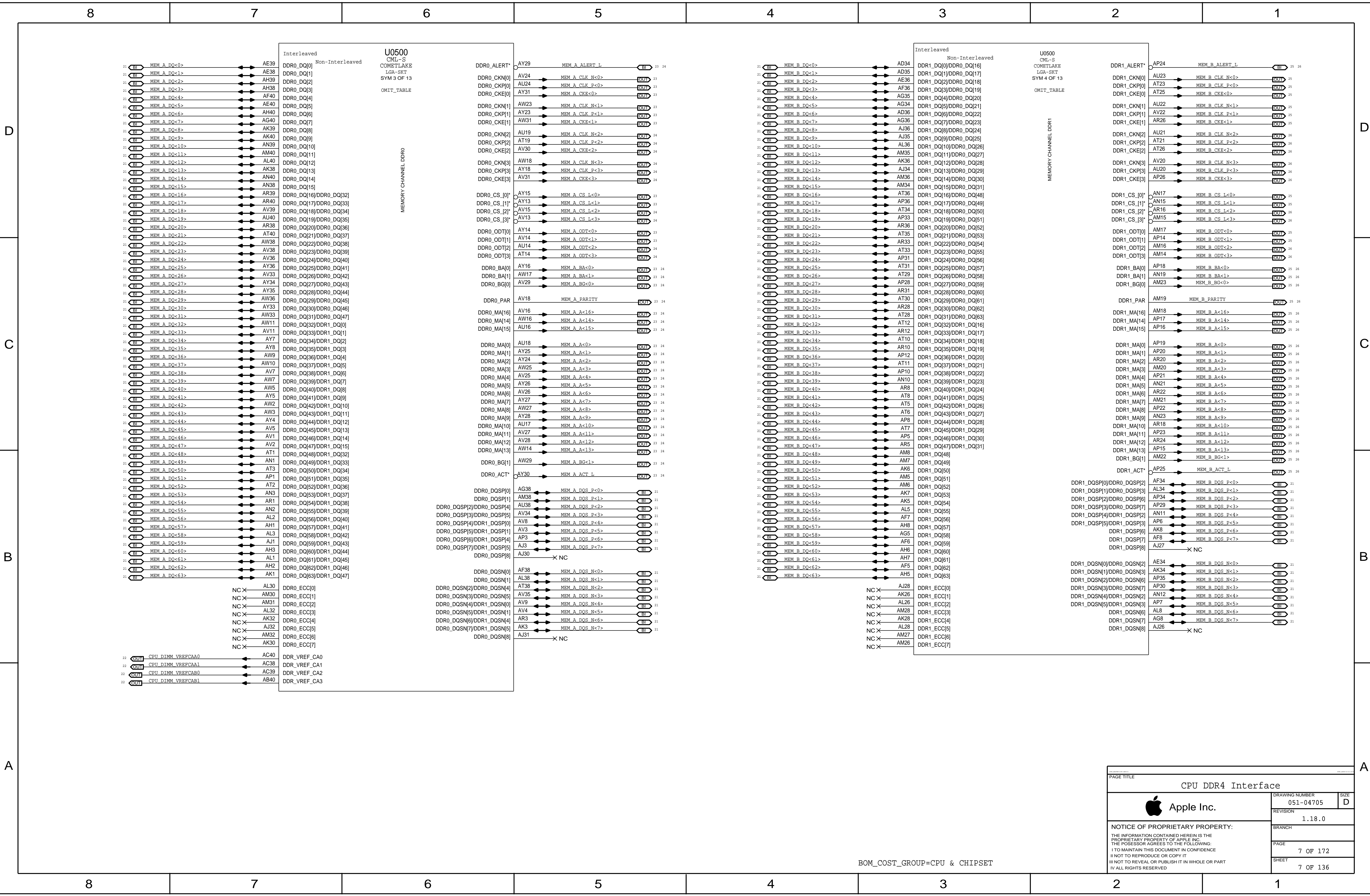
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DEBUG: LEDs			
	DRAWING NUMBER	051-04705	SIZE
	REVISION	1.18.0	D
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		PAGE	3 OF 172
		SHEET	3 OF 136

BOM_COST_GROUP=DEBUG



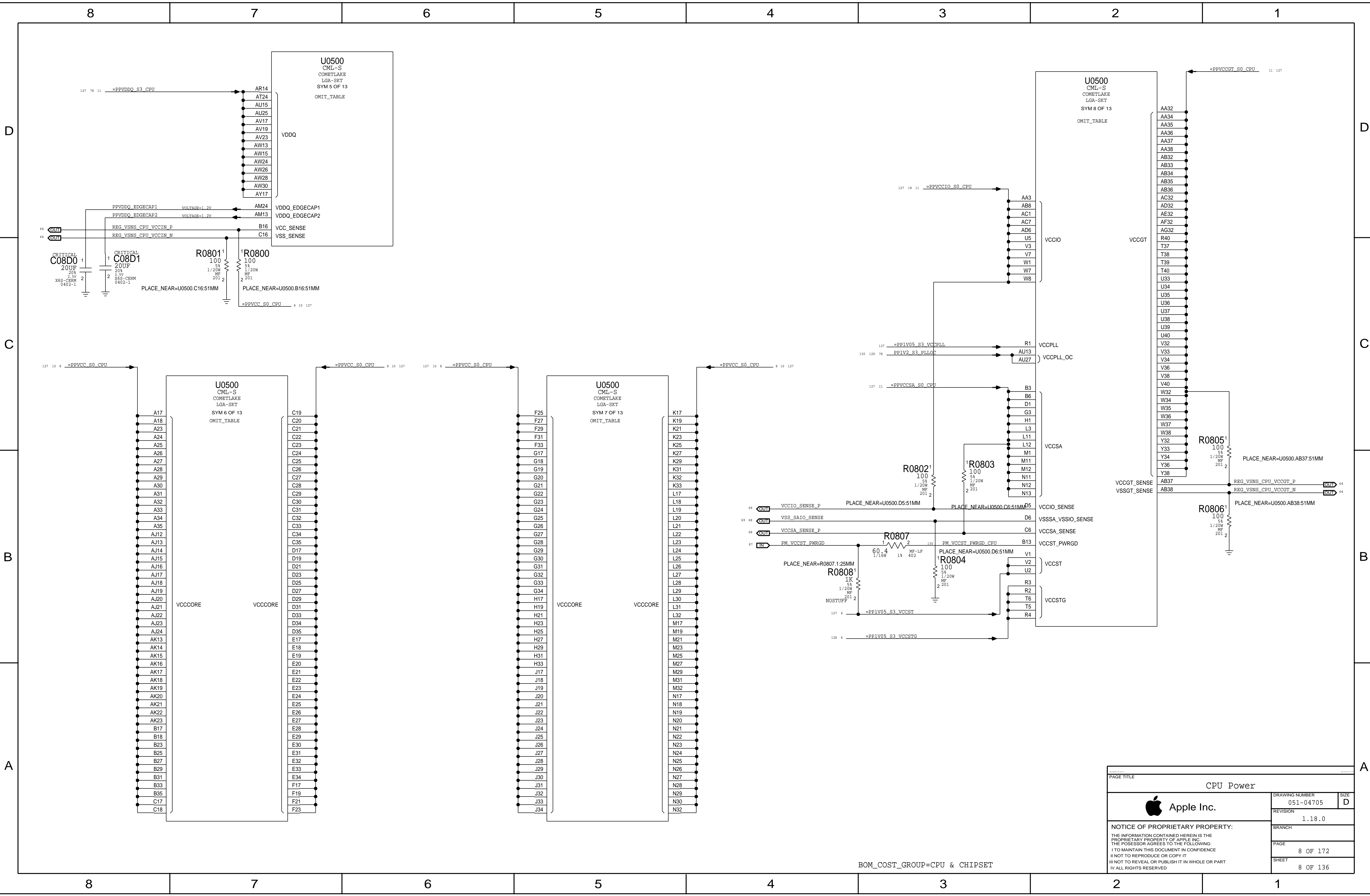
PAGE TITLE			
CPU DMI/PEG/DDI			
 Apple Inc.	DRAWING NUMBER	051-04705	SIZE D
	REVISION	1.18.0	
	BRANCH		
	PAGE	5 OF 172	
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BOM_COST_GROUP=CPU & CHIPSET



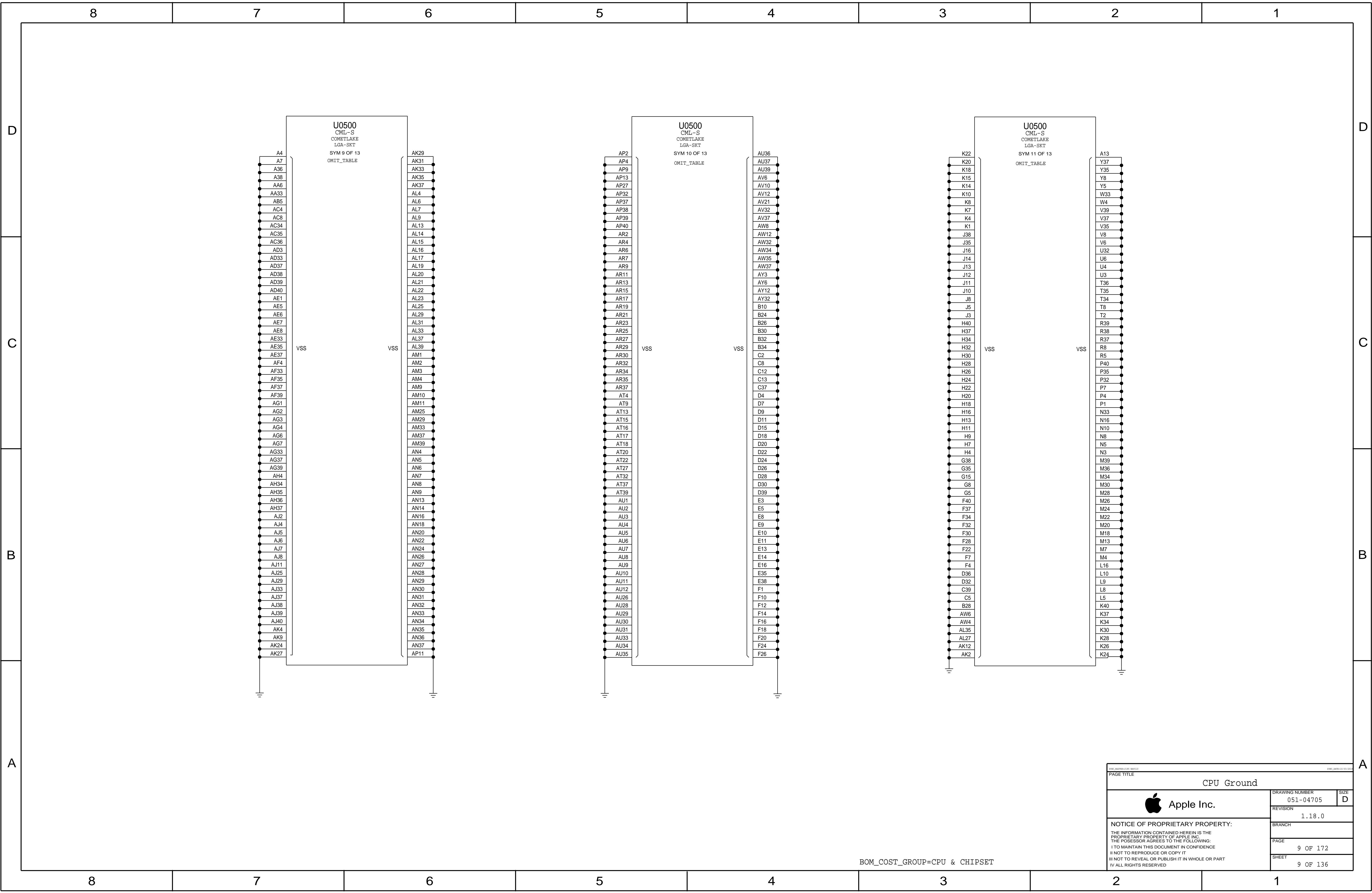
PAGE TITLE		
CPU DDR4 Interface		
	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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BOM_COST_GROUP=CPU & CHIPSET



PAGE TITLE		
CPU Power		
 Apple Inc.	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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BOM_COST_GROUP=CPU & CHIPSET

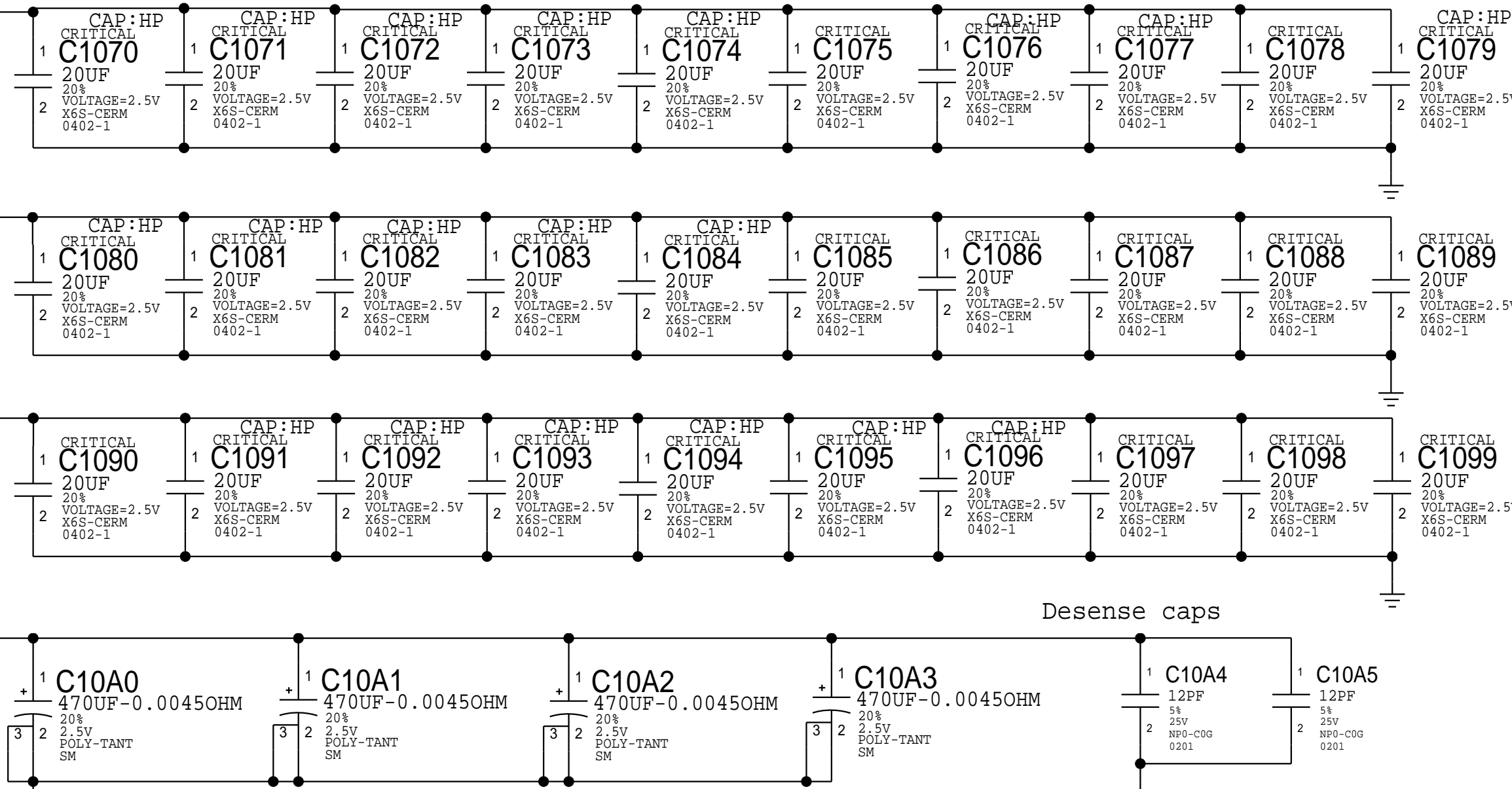



PAGE TITLE		
CPU Ground		
 Apple Inc.	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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BOM_COST_GROUP=CPU & CHIPSET

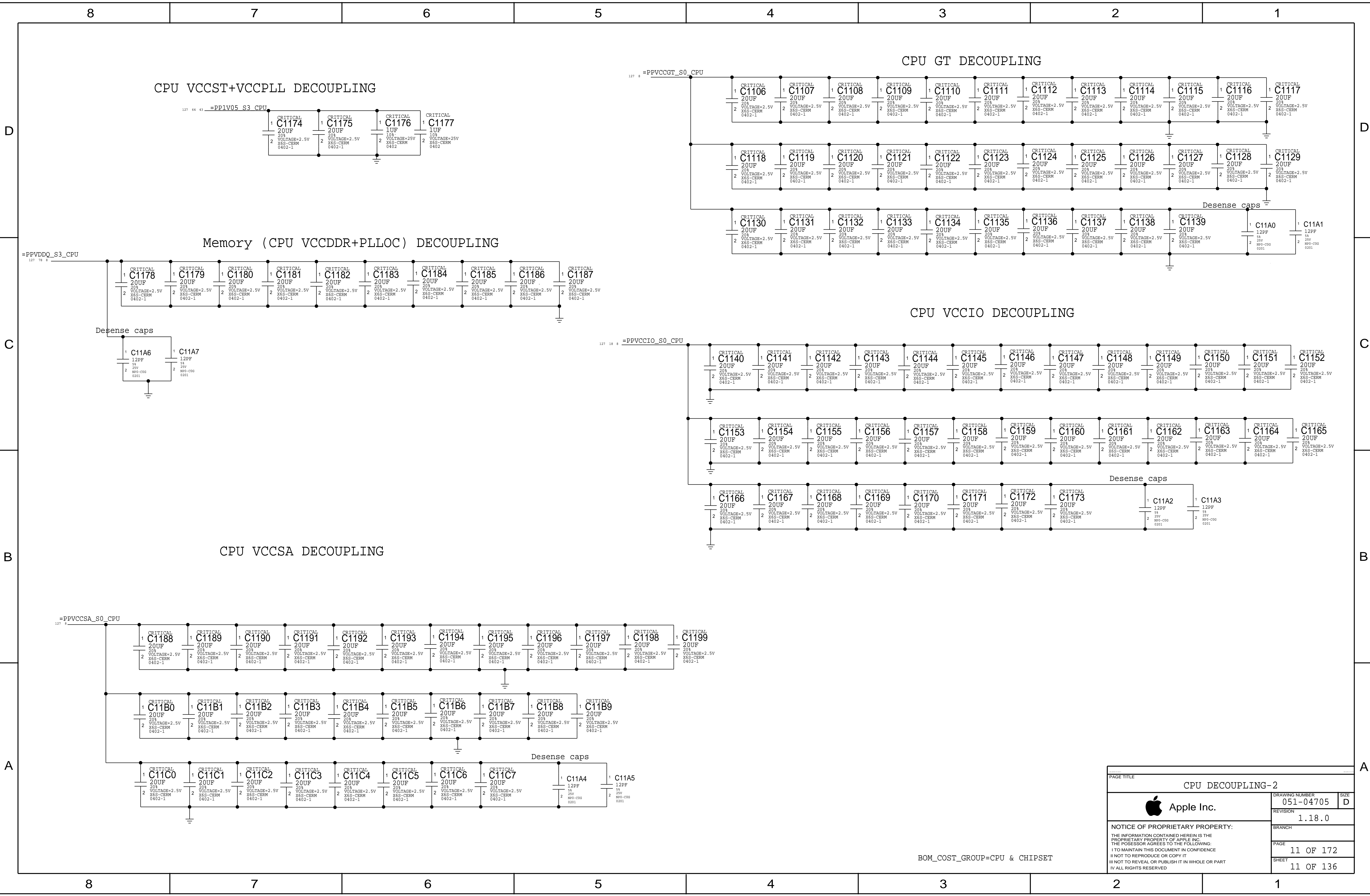
CPU VCORE DECOUPLING


127 8 =PPVCC_S0_CPU



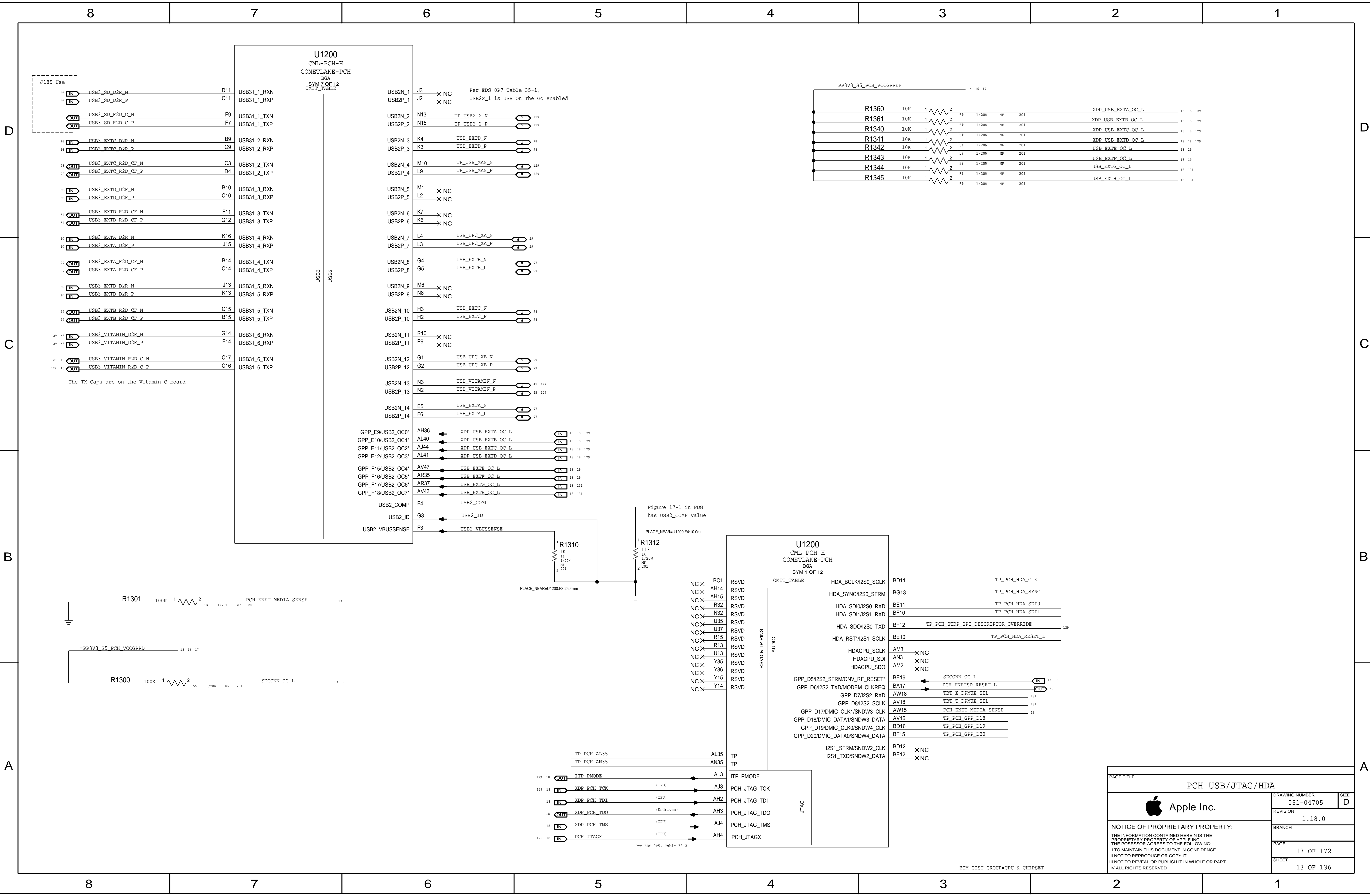
PAGE TITLE		
CPU DECOUPLING 1		
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	SHEET	10 OF 136

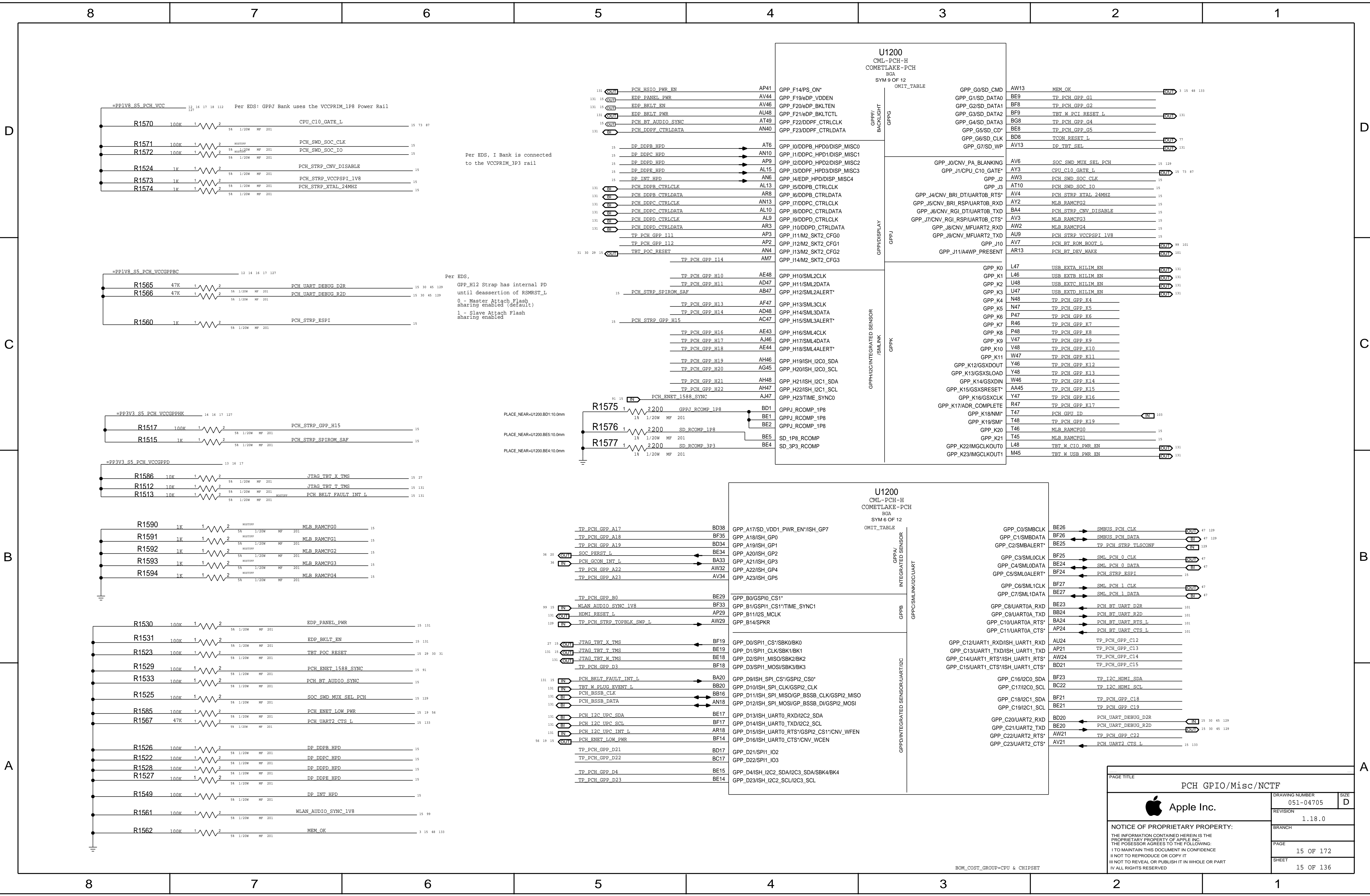
BOM_COST_GROUP=CPU & CHIPSET



PAGE TITLE		
CPU DECOUPLING-2		
 Apple Inc.	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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BOM_COST_GROUP=CPU & CHIPSET





D

C

B

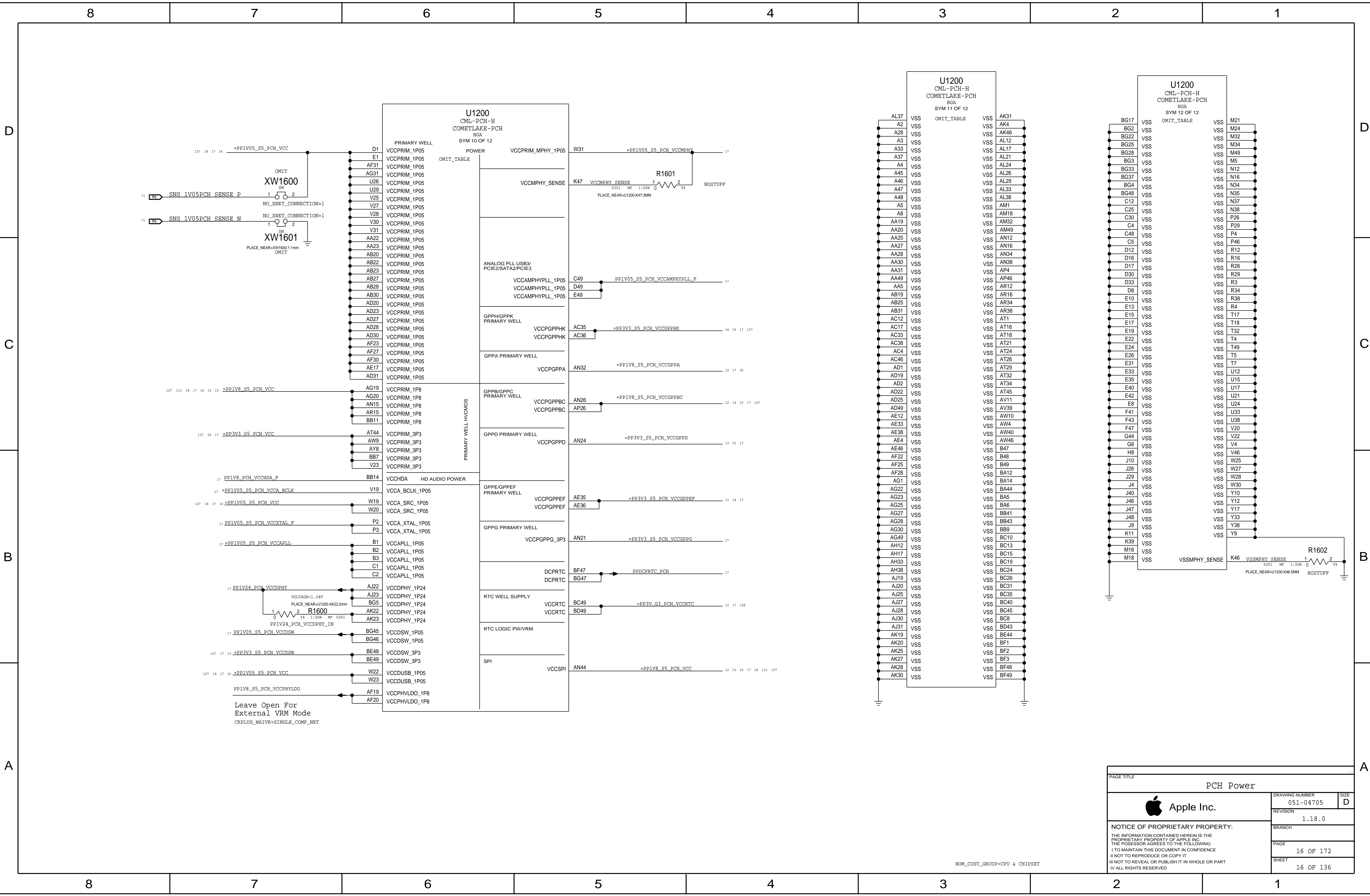
A


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PAGE TITLE		
PCH Power		
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	REVISION	1.18.0
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SHEET		
16 OF 136		

BOM_COST_GROUP=CPU & CHIPSET

D

C

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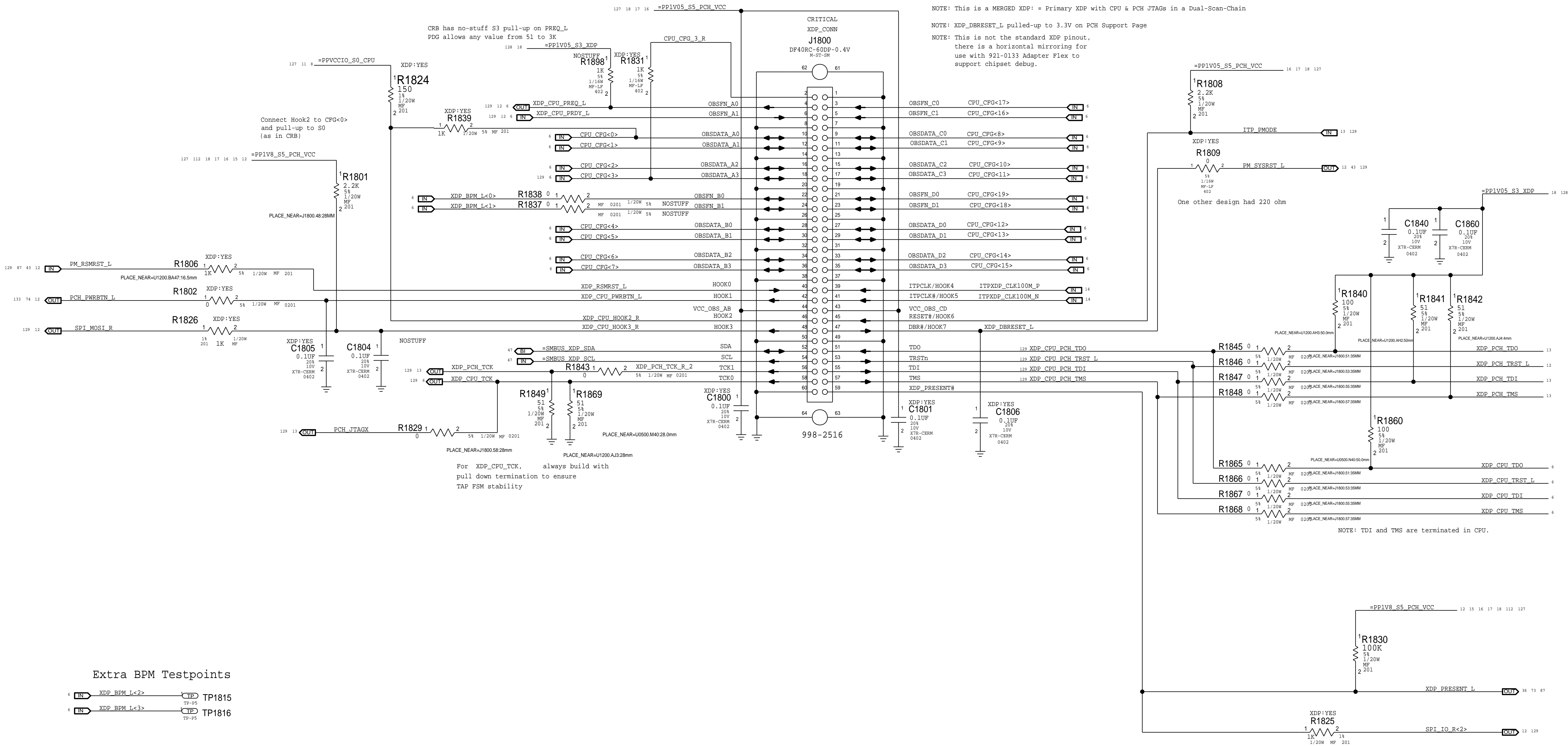
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Micro2-XDP



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE		
CPU XDP		
 Apple Inc.	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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	PAGE	18 OF 172
	SHEET	18 OF 136

D

C

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A

D

C

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A

8

7

6

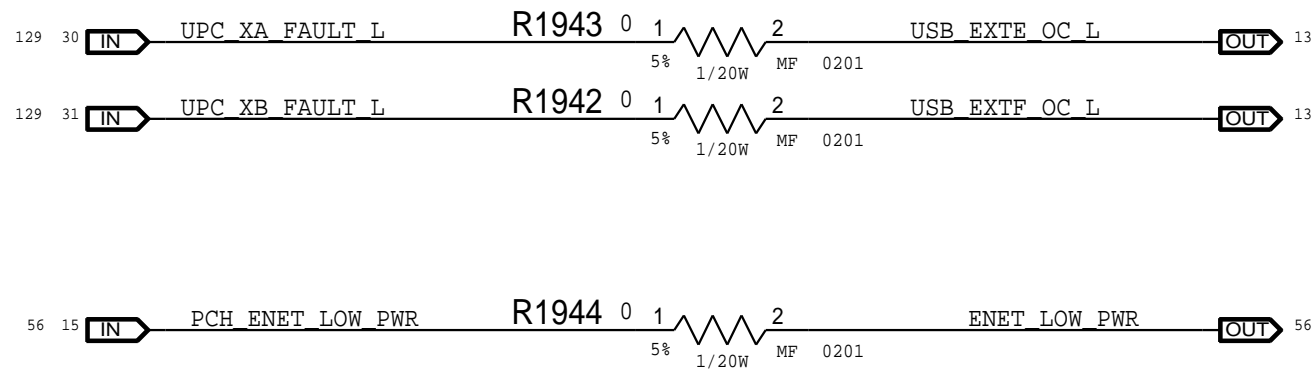
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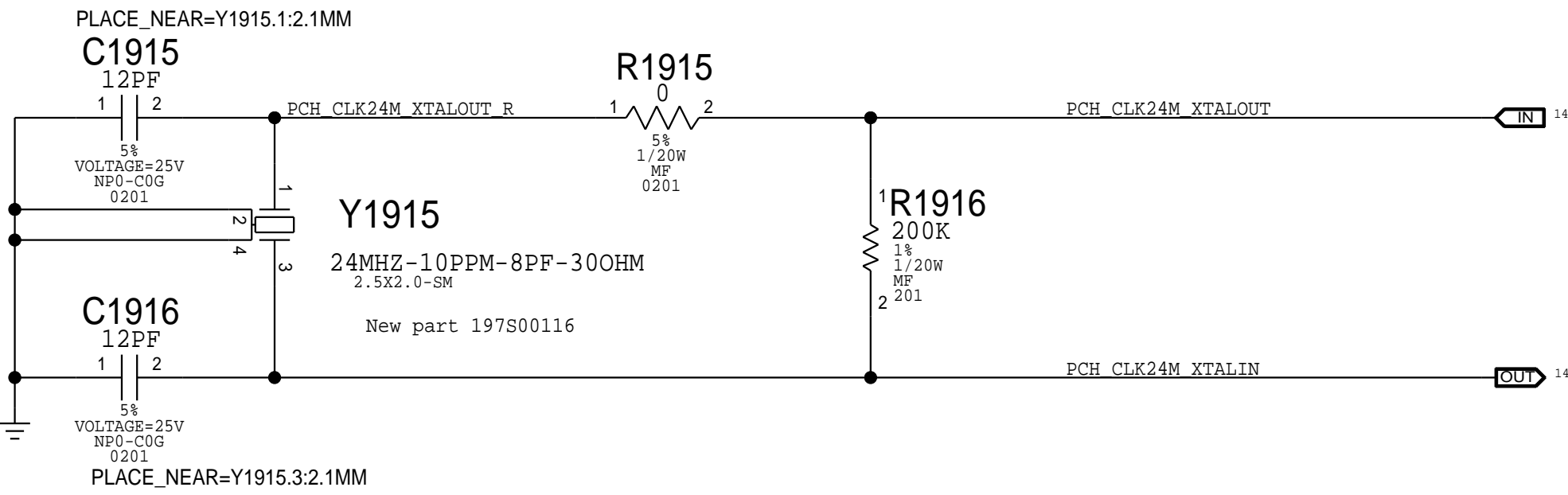
3

2

1

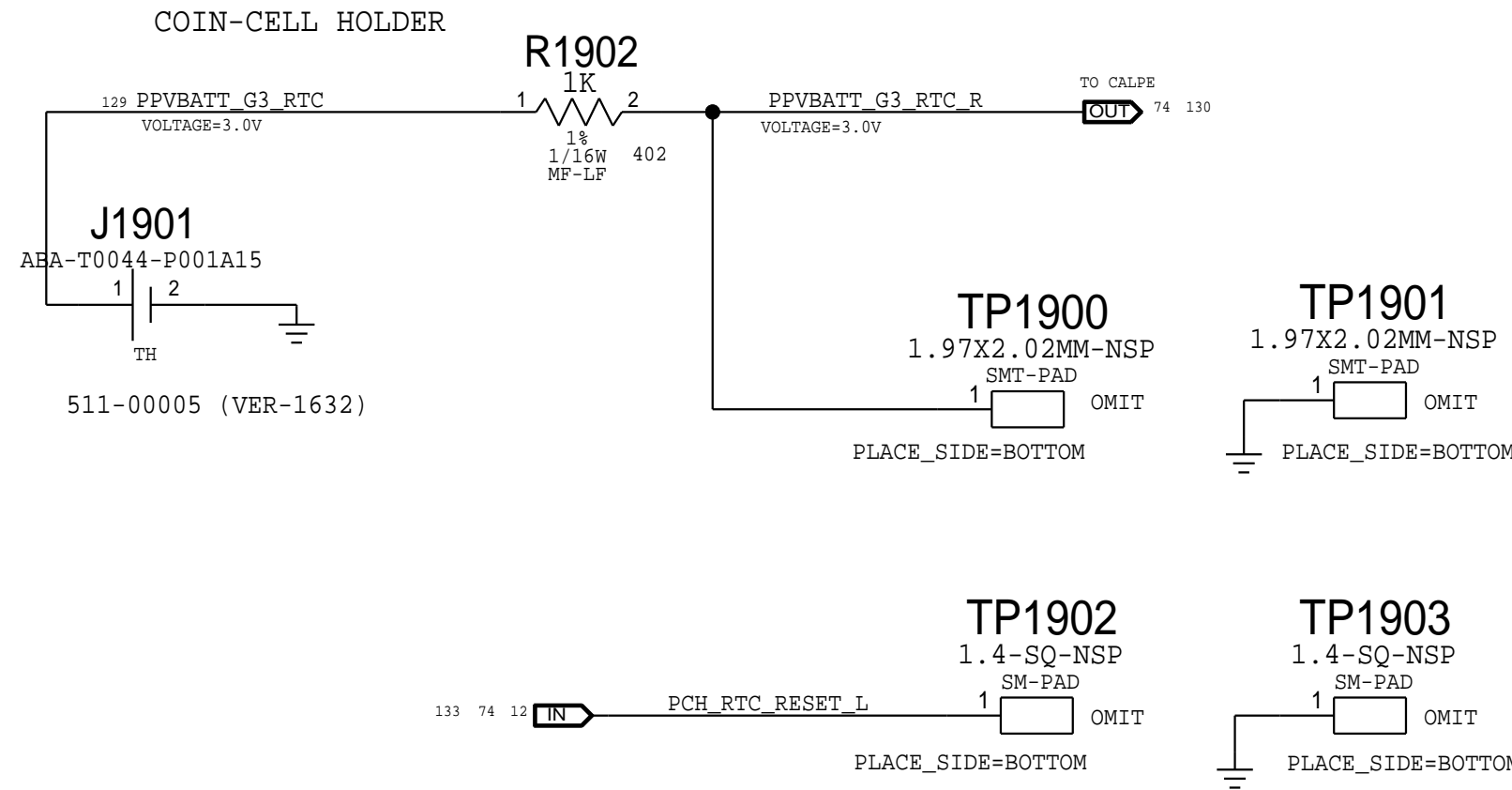


PCH 24MHz Crystal




Ce = 2 * [C1 - (Cs + Ci)]
C1 per 197S00116 spec = 8pf
Cs is trace and xtal pad capacitance ~= 1pf (extract after layout)
Ci is PCH pin capacitance ~= 1 pf (assumption, need spec)
Ce = 2 * [8 - (1 + 1)] = 2 * [8 - 2] = 2 * 6 = 12 pf

RTC Power Sources

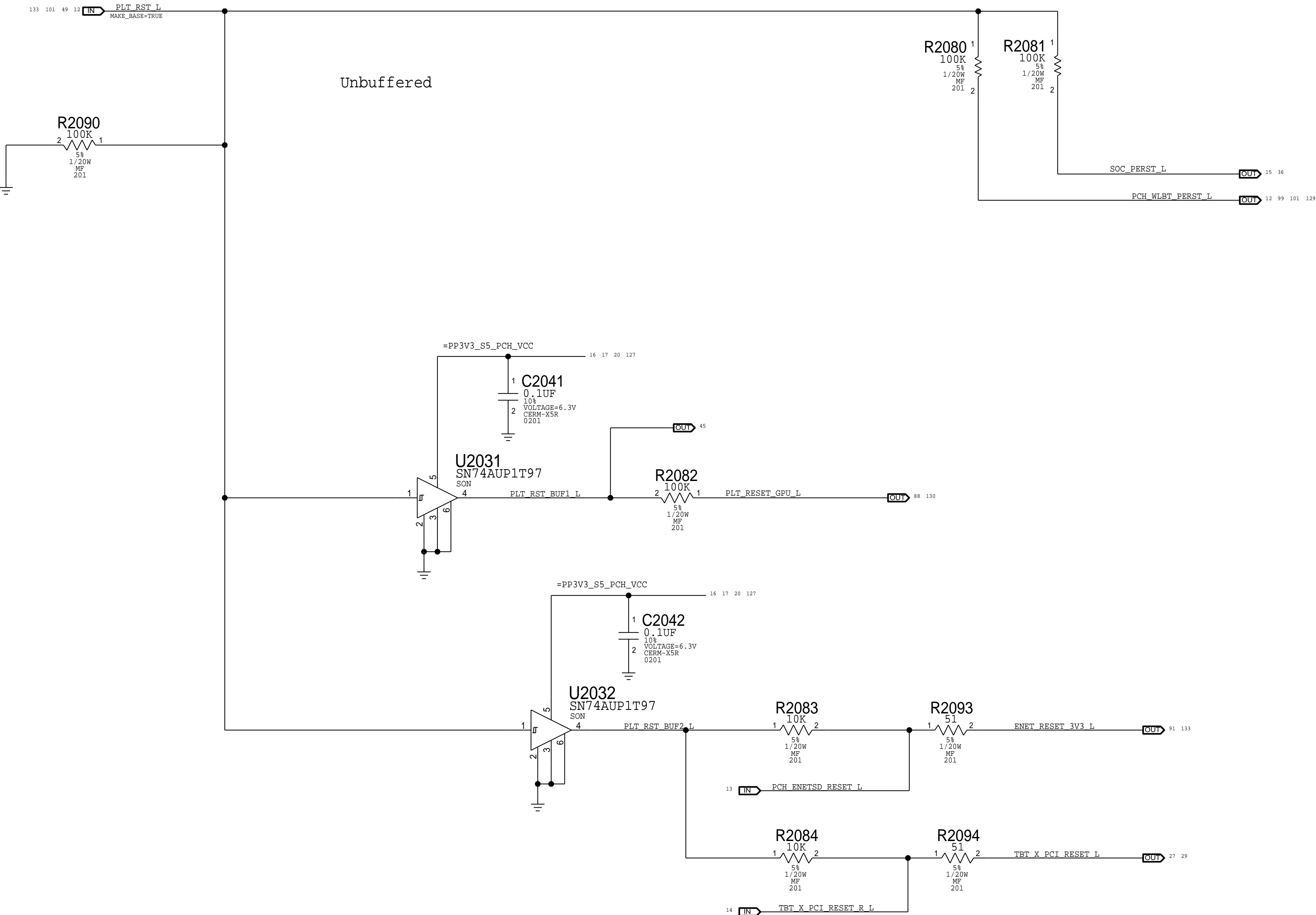


Place TP1901-TP1903 on bottom side


BOM_COST_GROUP=CPU & CHIPSET

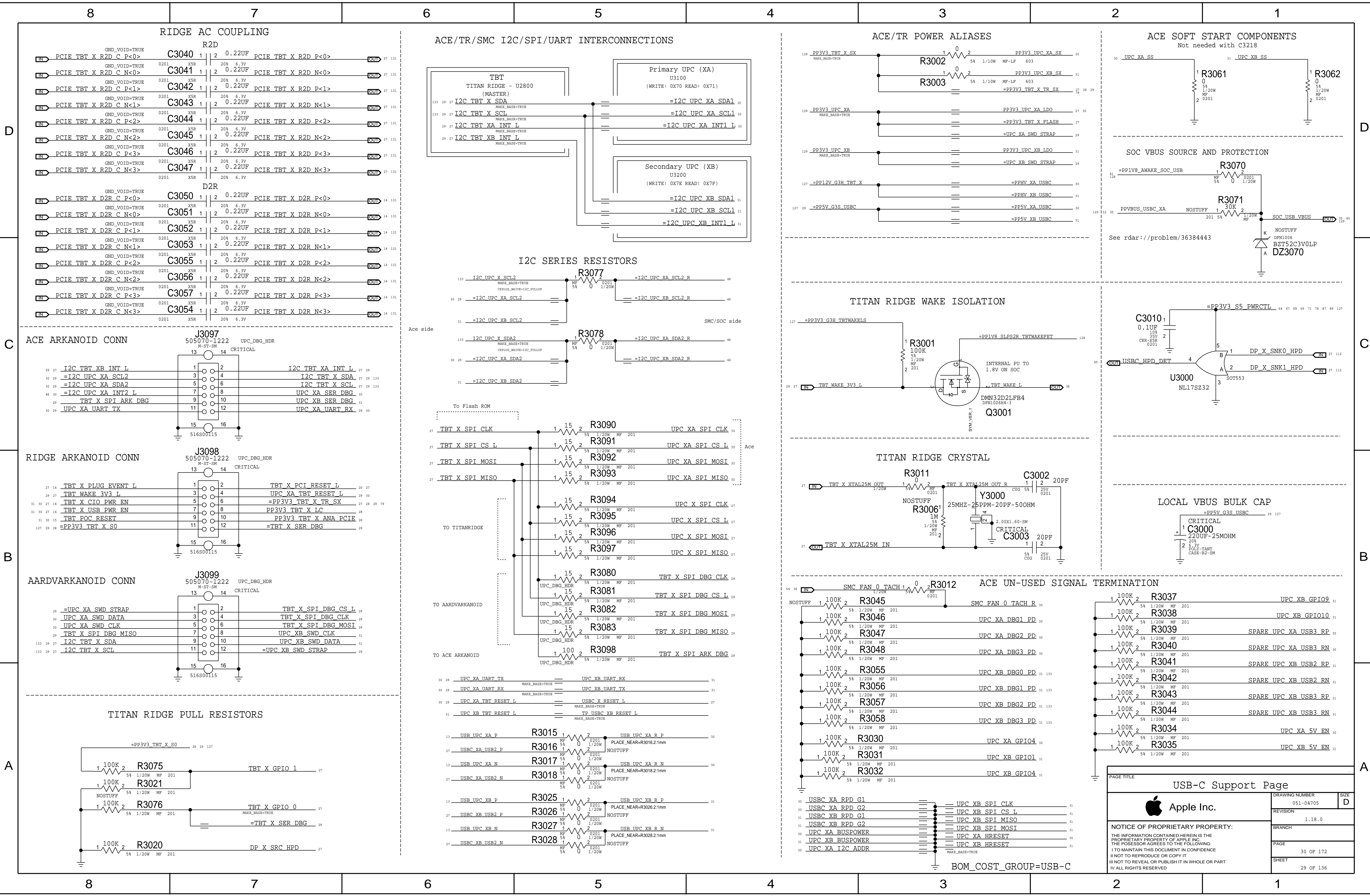
PAGE TITLE		
CPU & CHIPSET: Chipset Support		
 Apple Inc.	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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MOW NOTE WW34
SECTION 5.1.4



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE		
Project-Specific Chipset Support		
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X SECONDARY ACE USB-C PORT CONTROLLER (UPC)

ACE2 PINCONFIG
(1) 3.3V PP
(2) 3.3V OD NMOS
(3) 3.3V OD PMOS
(4) 3.3V INPUT
(5) 1.8V PP
(6) 1.8V OD NMOS
(7) 1.8V OD PMOS
(8) 1.8V INPUT

ACE LDO CAN DRAW UP TO
5.9 MA WHILE PROGRAMMING OTP
MAX 100UF TOTAL ON RAIL

=PPHV_XB_USBC

C3298
10UF
25V
X6S-CERM
0402

C3299
1.0UF
35V
CERM-X5R
0402

MRESET HIGH FORCES B17 RESET LOW
ACTIVE LOW RESET OUTPUT

TP must be present on GPIO0 or be accessible on connector even in production

PD GPIO4

USE GPIO8 FOR PMU RESET AFTER BOOT

BUSPOWER needs to connect to GND on Desktop and LDO_3V3 on Mobile.
I2C_ADDR CONTROLS ADDR BITS 3,2,1
GND I2C_ADDR ON PRIMARY ONLY
R_0SC NEEDS NEEDS 0.1% RES

I2C BUS 1 IS TBT / ACES

I2C BUS 2 IS SMC / ACES

R3203
1.5K
1/20W
TF-LE
0201

TO SMC

L3200

PLACE_NEAR=U3200.H19:5mm

PLACE_NEAR=U3200.H21:5mm

90-OHM-0.1A

R3250

R3251

UPC_XB_HRESET B13
TBT_POC_RESET A14
UPC_XB_TBT_RESET_L B17
UPC_XB_SER_DBG A2
UPC_XB_GPIO1 D1
TBT_X_CIO_PWR_EN F1
UPC_XB_5V_EN C2
UPC_XB_GPIO4 E2
UPC_XB_FAULT_L B3
TBT_X_USB_PWR_EN C4
SOC_DOCK_CONNECT D3
UPC_XB_FMU_RESET E4
UPC_XB_GPIO9 F3
UPC_XB_GPIO10 F7
UPC_XB_BUSPOWER A18
NC_UPC_XB_I2C_ADDR M19
UPC_XB_R_OSC M21
I2C_UPC_XB_DBG_CTL_SDA A16
I2C_UPC_XB_DBG_CTL_SCL B15
I2C_UPC_XB_SDA1 B5
I2C_UPC_XB_SCL1 A4
I2C_UPC_XB_INT1_L D7
I2C_UPC_XB_SDA2 B7
I2C_UPC_XB_SCL2 A6
I2C_UPC_XB_INT2_L C8
UPC_XB_SPI_CLK B9
UPC_XB_SPI_MOSI B11
UPC_XB_SPI_MISO A10
UPC_XB_SPI_CS_L A8
UPC_XB_SWO_DATA E20
UPC_XB_SWO_CLK E16
UPC_XB_UART_RX B19
UPC_XB_UART_TX A20
USB_UPC_XB_F_P H19
USB_UPC_XB_F_N H21
SPARE_UPC_XB_USB2_RP G20
SPARE_UPC_XB_USB2_RN G22
SPARE_UPC_XB_USB3_RP F19
SPARE_UPC_XB_USB3_RN F21
USBC_XB_AUXLSX1 J12
USBC_XB_AUXLSX2 H11
DP_XB_HPD C12
UPC_XB_DBG0_PD G12
UPC_XB_DBG1_PD F11
UPC_XB_DBG2_PD E8
UPC_XB_DBG3_PD E12
UPC_XB_DBG4 G16
UPC_XB_DBG5 F15
SMC_DEBUGPRT_TX D15
SMC_DEBUGPRT_RX D19

HRESET
MRESET
RESET*
GPIO0 (1)
GPIO1 (X)
GPIO2 (4)
GPIO3 (3)
GPIO4 (X)
GPIO5 (4)
GPIO6 (4)
GPIO7 (7)
GPIO8 (7)
GPIO9 (X)
GPIO10 (X)
BUSPOWER
I2C_ADDR
R_OSC
I2CM_SDA_CNFG
I2CM_SCL_CNFG
I2C_SDA1
I2C_SCL1
I2C_IRQ1* OD
I2C_SDA2
I2C_SCL2
I2C_IRQ2* OD
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
SWO_DATA
SWO_CLK
UART_RX
UART_TX
USB_RP1_P
USB_RP1_N
USB_RP2_P
USB_RP2_N
USB_RP3_P
USB_RP3_N
AUX_P
AUX_N
HPD
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG6
DEBUG7

U3200
CD32172B11ACE
FCBGA
CRITICAL
ONKIT_PABLE

DIGITAL CORE I/O & CONTROL

POWER

TYPE-C

PORT_MUX

GND

GND
A22
H9
N20
B21
K15
N22

VIN_3V3 C20
VDDIO A12
VDDIO_CFG D11
LDO_3V3 (D21
VIN_LV L20
VOUT_LV L18
VRET C16
SS L22
LDO_CORE E22
VBUS_OPT D5
PP_HV_OPT F5

PPV3V3_USBC_XB
PPV3V3_G3H_UPC_XB
PP3V3R1V8_UPC_XB
PP3V3_UPC_XB_LDO
PP3V3_UPC_XB_SX
UPC_XB_SS
PP1V5_UPC_XB_LDO_CORE
PPV3V3_USBC_XB
=PPHV_XB_USBC
USBC_XB_CC1
USBC_XB_CC2
USBC_XB_RPD_G1
USBC_XB_RPD_G2
USBC_XB_USB_TOP_P
USBC_XB_USB_TOP_N
USBC_XB_USB_BOT_P
USBC_XB_USB_BOT_N
USBC_XB_SBU1
USBC_XB_SBU2


C20
A12
D11
D21
L20
L18
C16
L22
E22
D5
F5
M15
N16
M17
N18
L14
L16
K19
K21
J20
J22
J16
H15

C18
E18
D17
G18

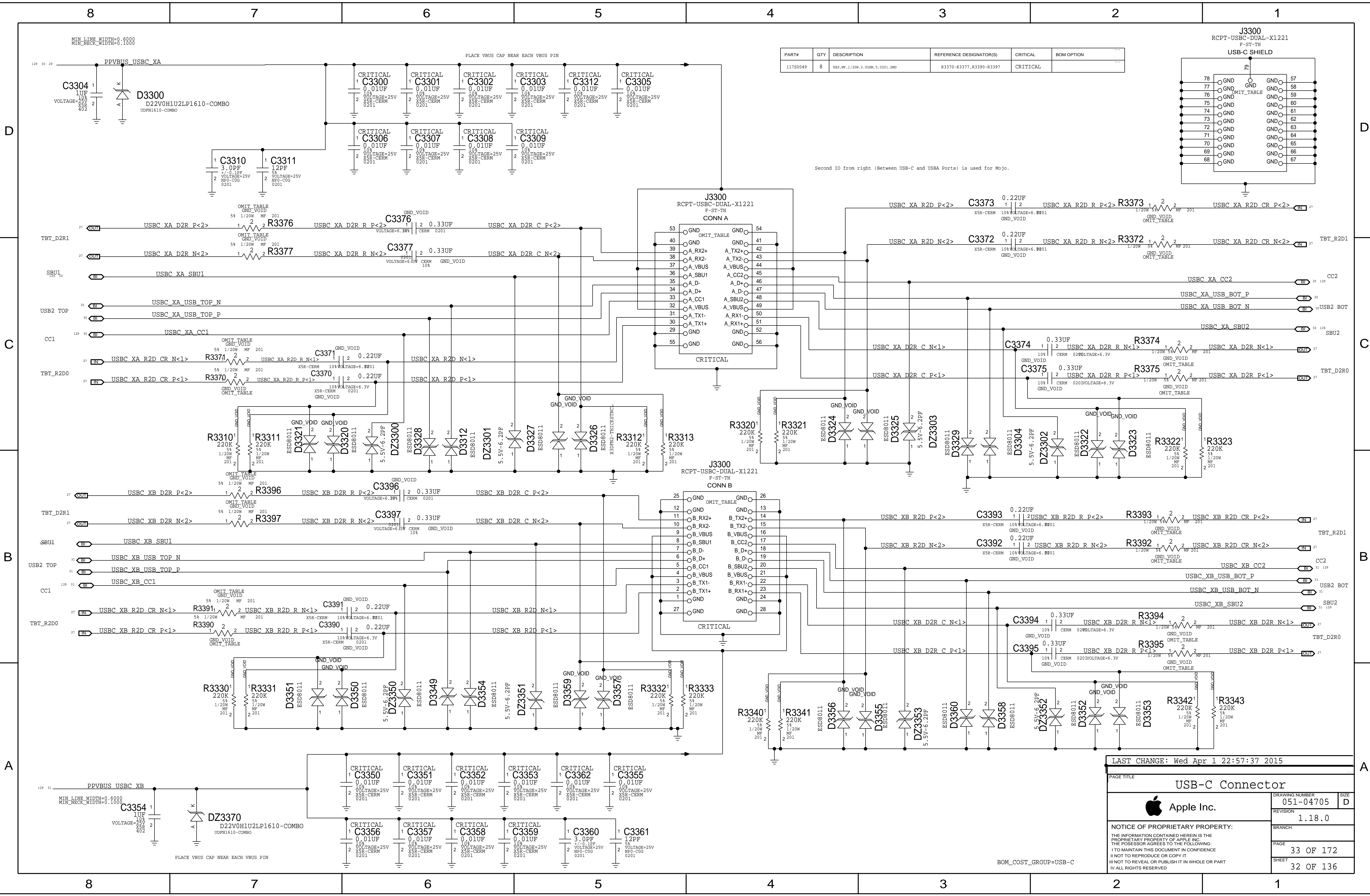
PULL R3109 AND R3108 UP TO ACES LDO FOR 1ST RIDGE'S ACES
PULL THEM DOWN TO GND FOR 2ND RIDGE'S ACES

R3209 I2C_UPC_XB_DBG_CTL_SCL
R3208 I2C_UPC_XB_DBG_CTL_SDA

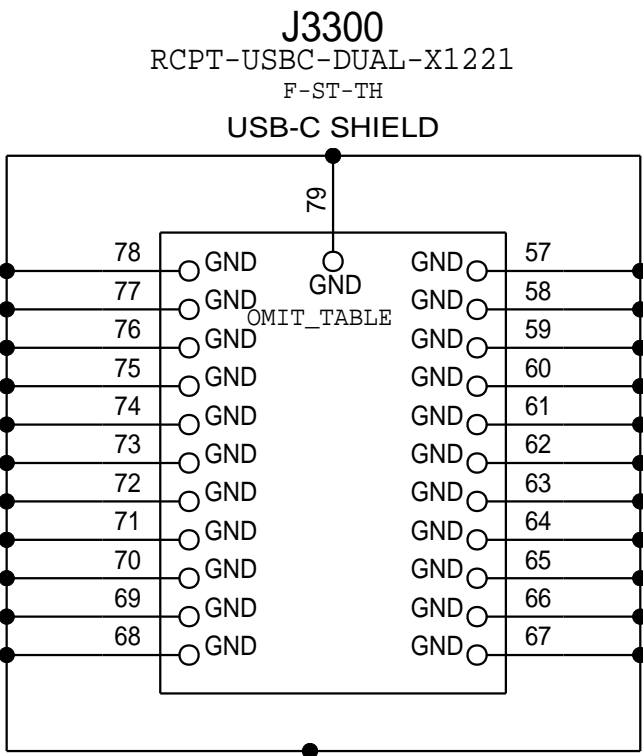
R3205 UP_CX_UART_RX

0105 HWV110			
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		PAGE	32 OF 172
		SHEET	31 OF 136

BOM_COST_GROUP=USBC-C



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0049	8	RBS,MF,1/20W,2.000M,5.0201,SMD	R3370-R3377,R3390-R3397	CRITICAL	



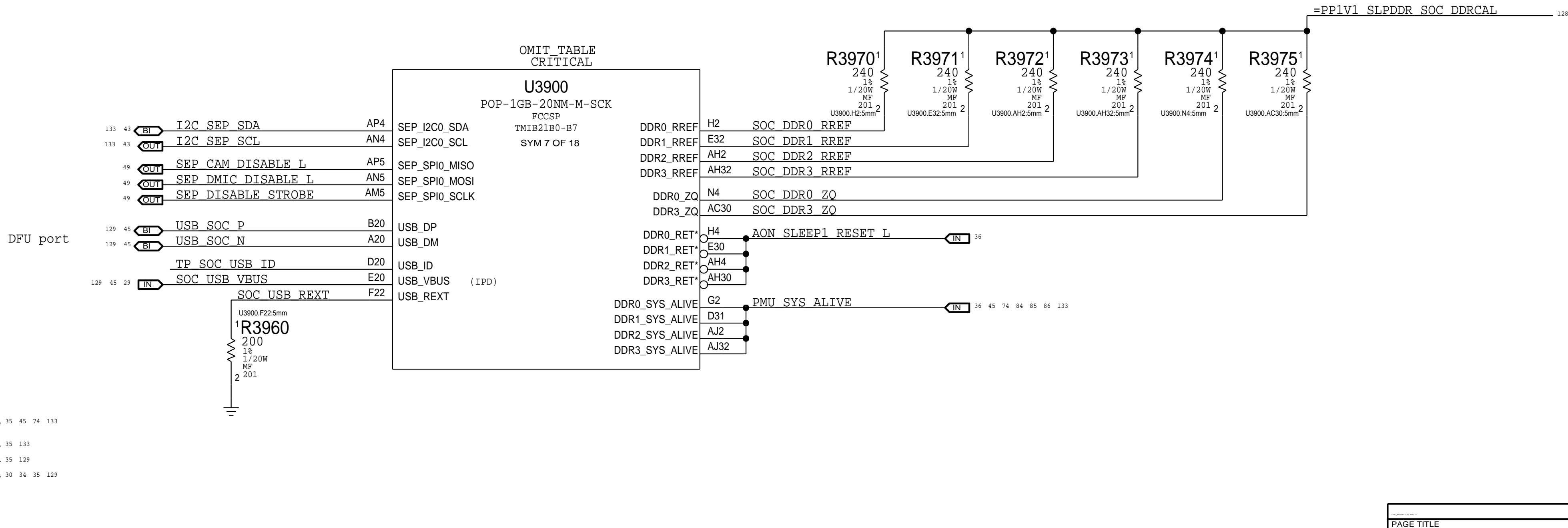
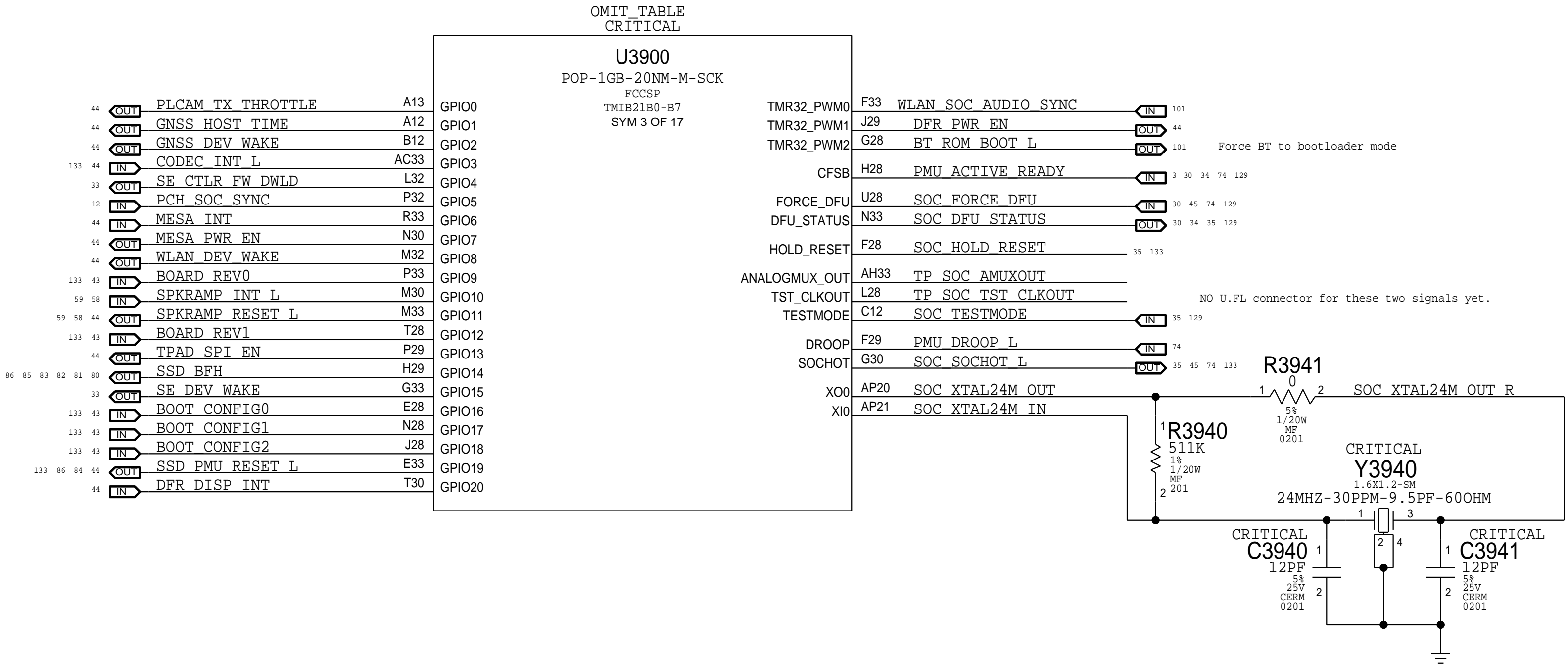
Second IO from right (Between USB-C and USB-A Ports) is used for Mojo.


LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE		USB-C Connector	
		DRAWING NUMBER	051-04705
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		PAGE	33 OF 172
		SHEET	32 OF 136

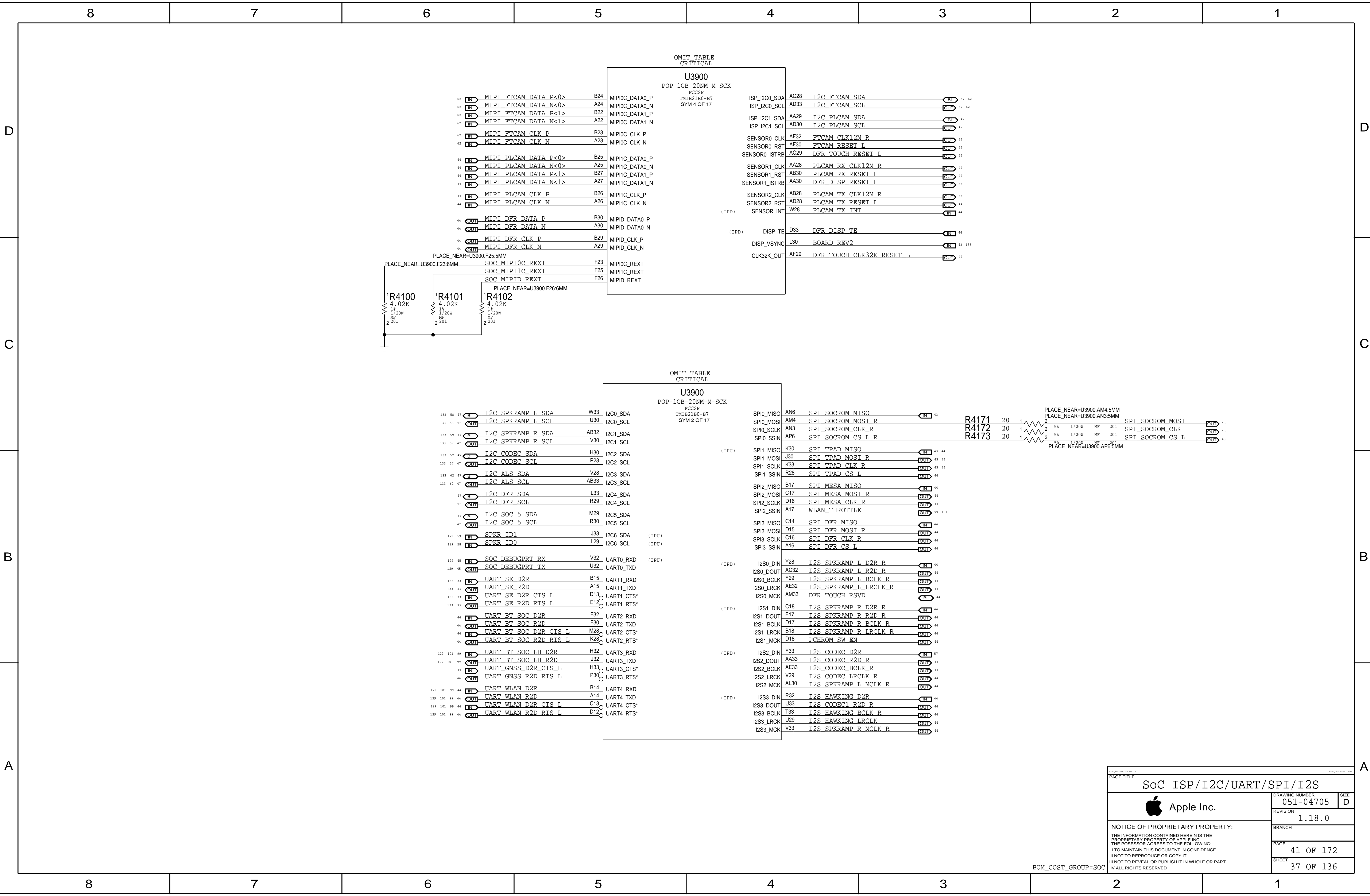
BOM_COST_GROUP=USB-C

Note 1) IPU represents SW configured state, not HW default



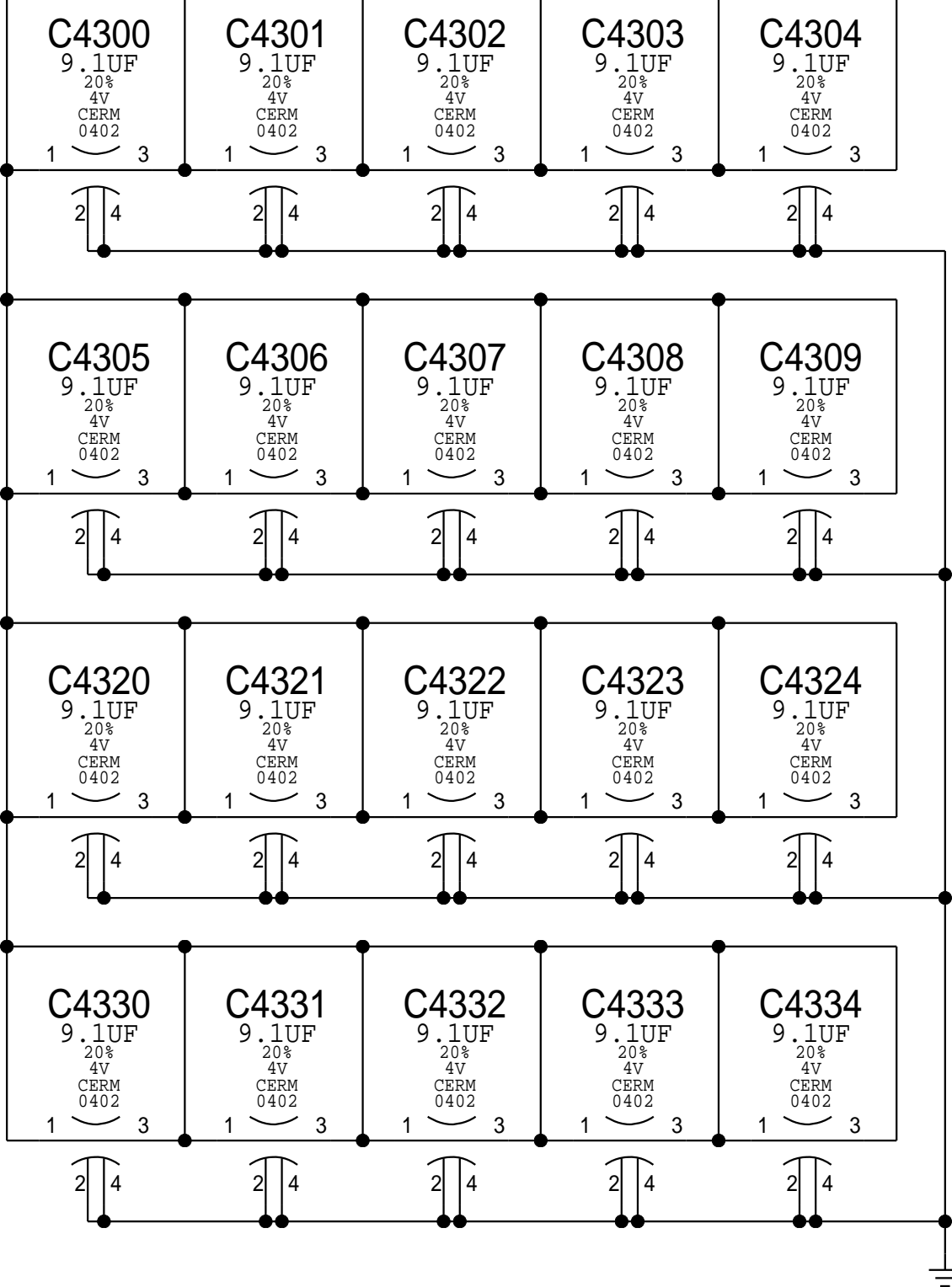
PAGE TITLE SoC GPIO/SEP/USB/DDR/Test		
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	REVISION 1.18.0	BRANCH
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PAGE 39 OF 172		
SHEET 35 OF 136		

BOM_COST_GROUP=SOC

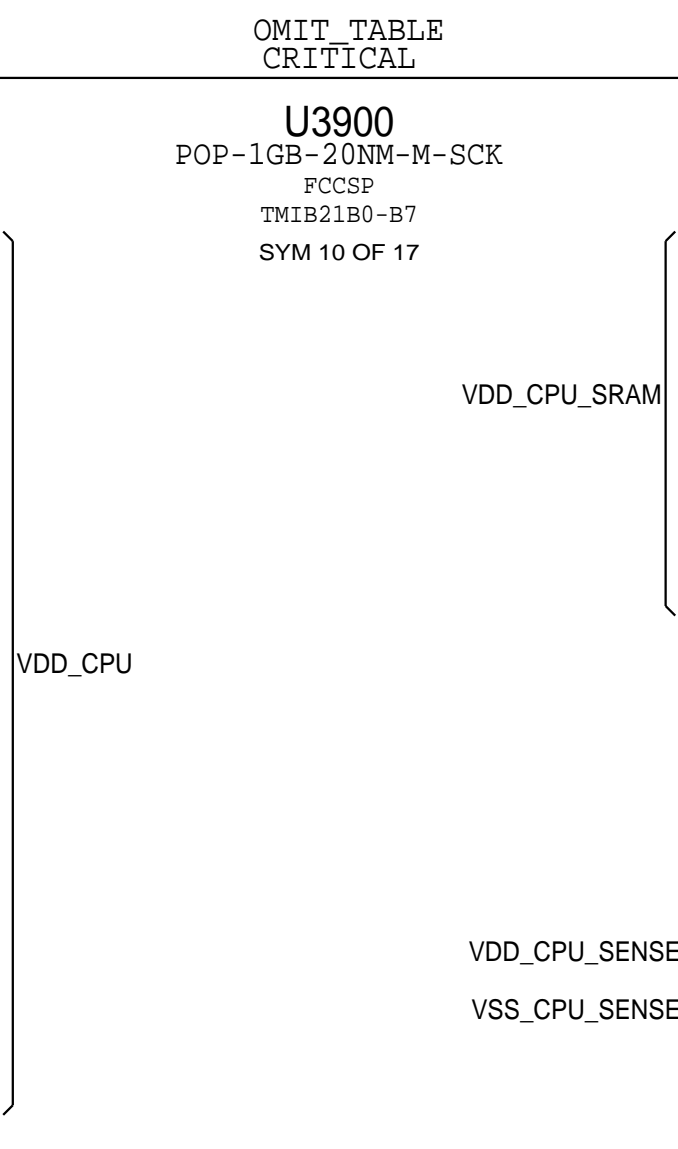


Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

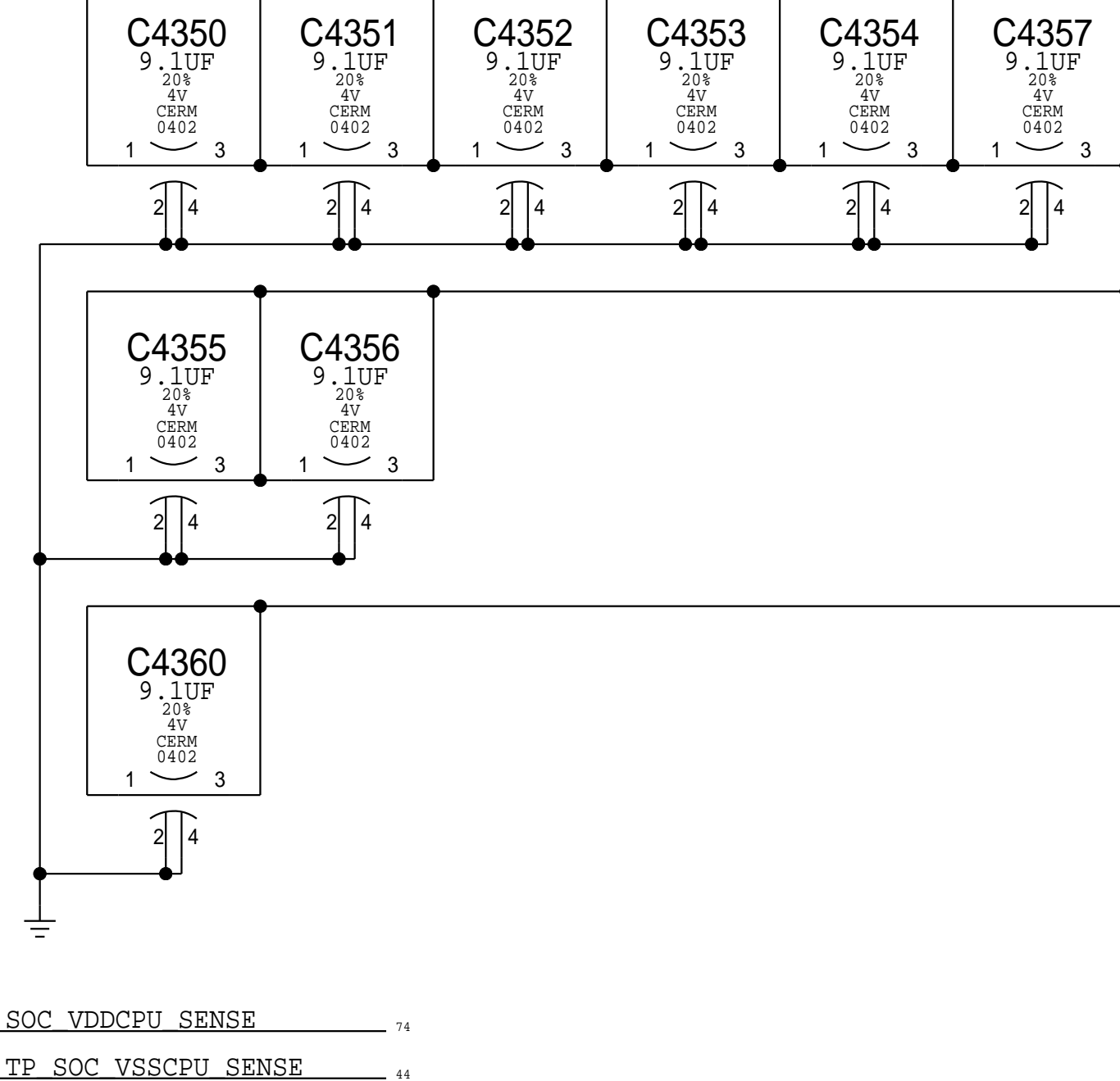
128 =PPVDDCPU AWAKE SOC
0.625V - 1.06V
11.6A Max



AA12
AA14
AA16
AB11
AB13
AB15
N12
N14
N16
P11
P13
P15
R10
R12
R14
U12
U14
U16
W10
W12
W14
Y11
Y13
Y15

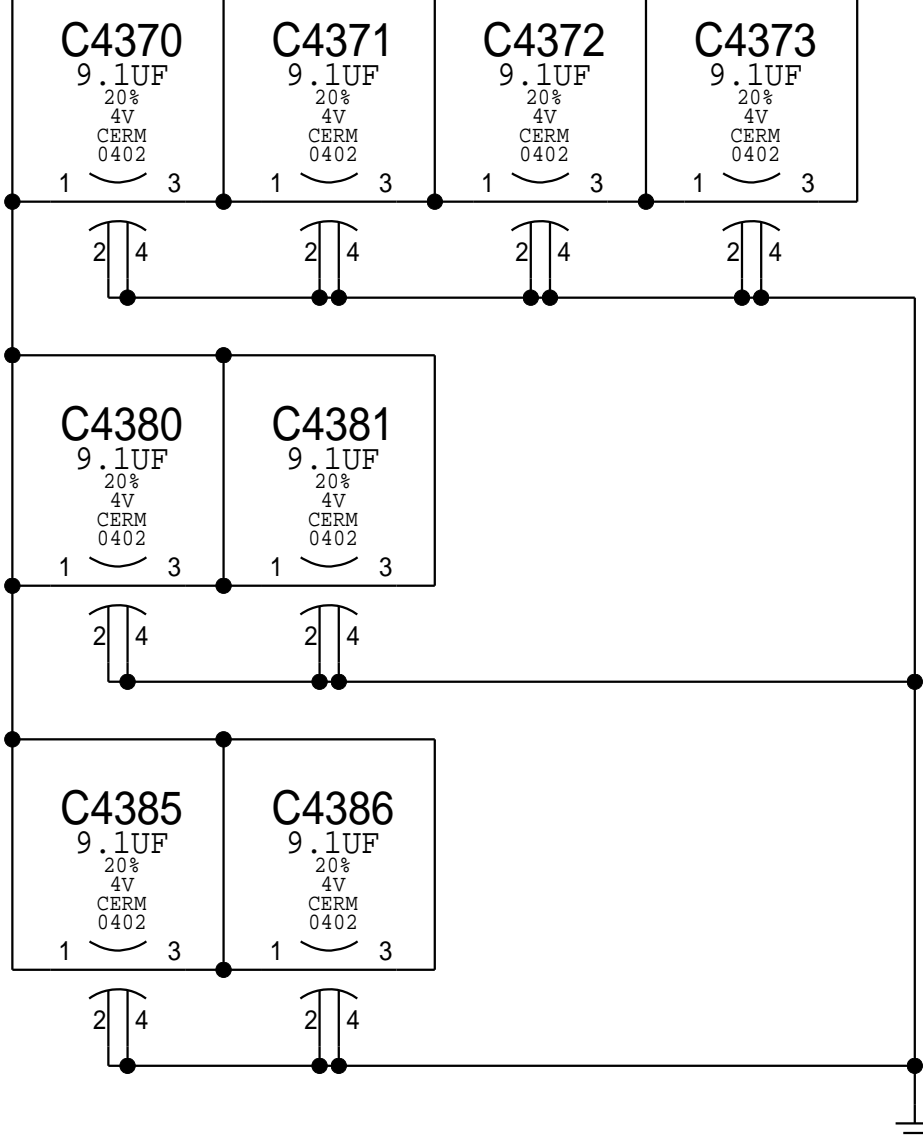


AA10
N10
R16
T11
T13
T15
U10
V11
V13
V15
W16

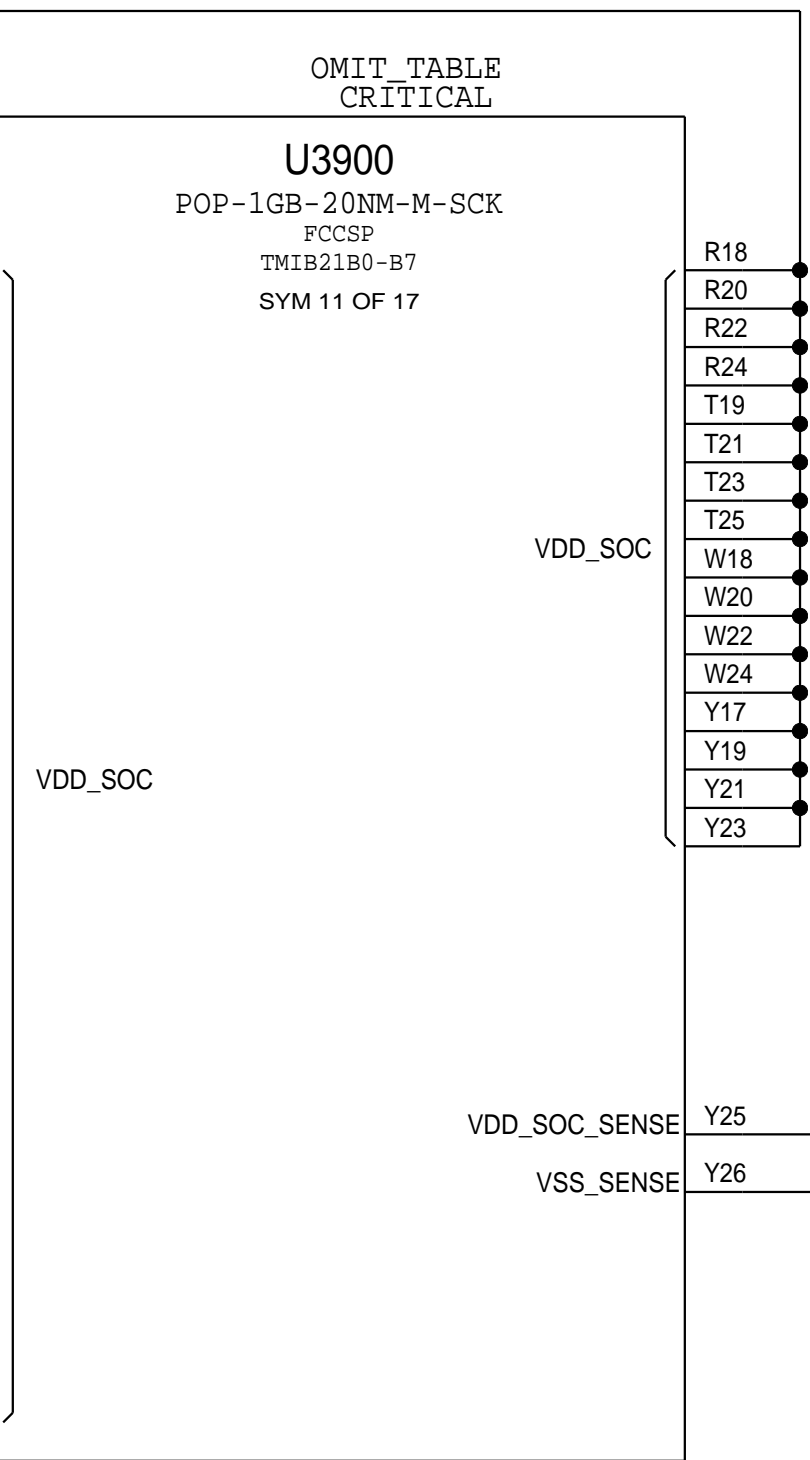


128 =PPVDDCPU AWAKE SOC
0.8V - 1.06V
0.9A Max

128 =PPOV82_SLPDDR VDDSOC
5.6A Max




AC10
AC12
AC14
AC16
AC18
AC20
AC22
AC24
AD11
AD13
AD15
AD17
AD19
AD21
AD23
AD25
L10
L12
L14
L16
L18
L20
L22
L24
M11
M13
M15
M19
M21
M23
M25



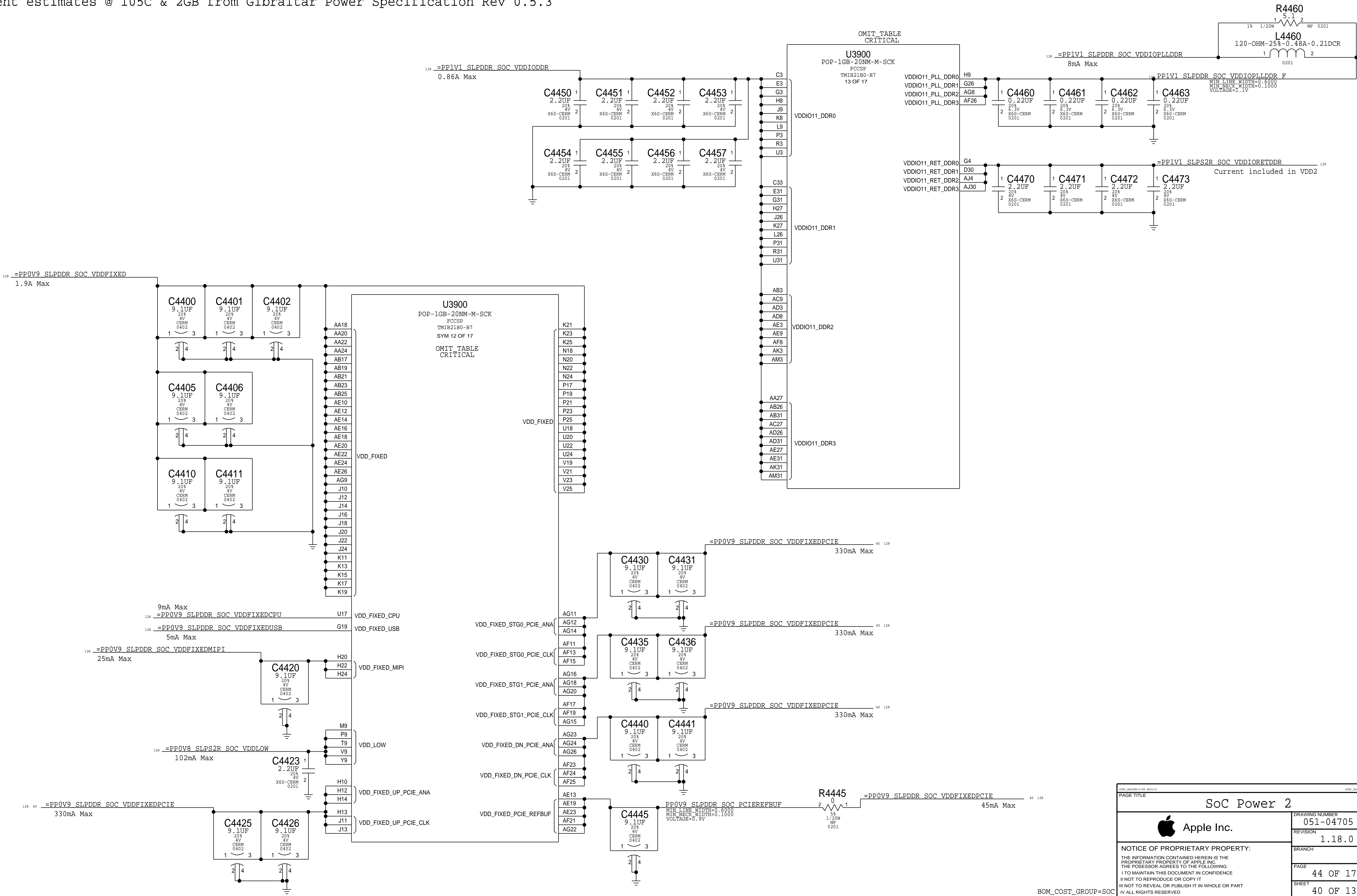
R18
R20
R22
R24
T19
T21
T23
T25
W18
W20
W22
W24
Y17
Y19
Y21
Y23

Y25 TP_SOC VDDSOC_SENSE
Y26 TP_SOC VSSSOC_SENSE

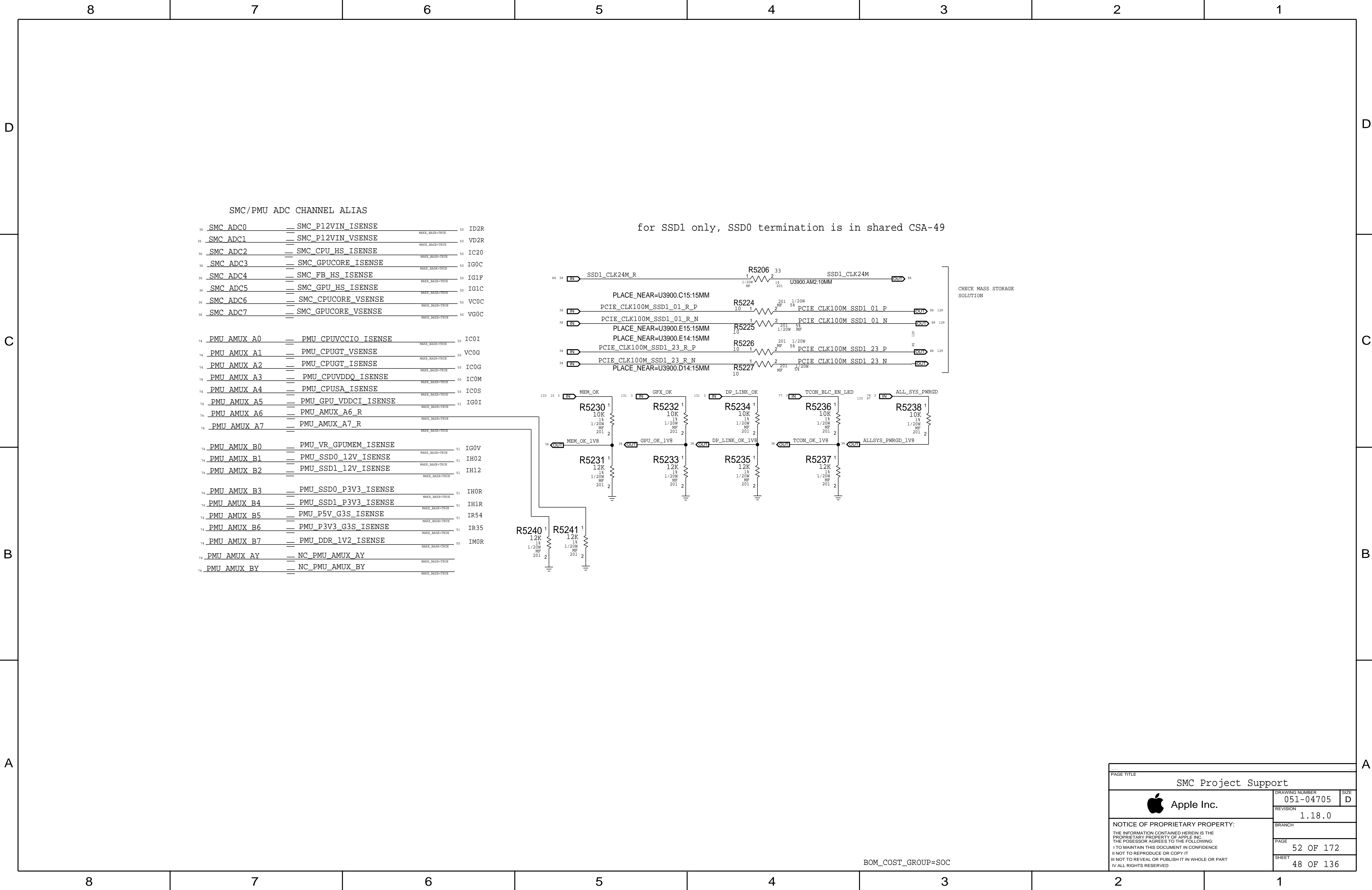
PAGE TITLE		
SoC Power 1		
 Apple Inc.	DRAWING NUMBER	051-04705
	REVISION	1.18.0
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BOM_COST_GROUP=SOC

Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



PAGE TITLE			
SoC Power 2			
	DRAWING NUMBER	051-04705	SIZE
	REVISION	1.18.0	
	BRANCH		
	PAGE	44 OF 172	
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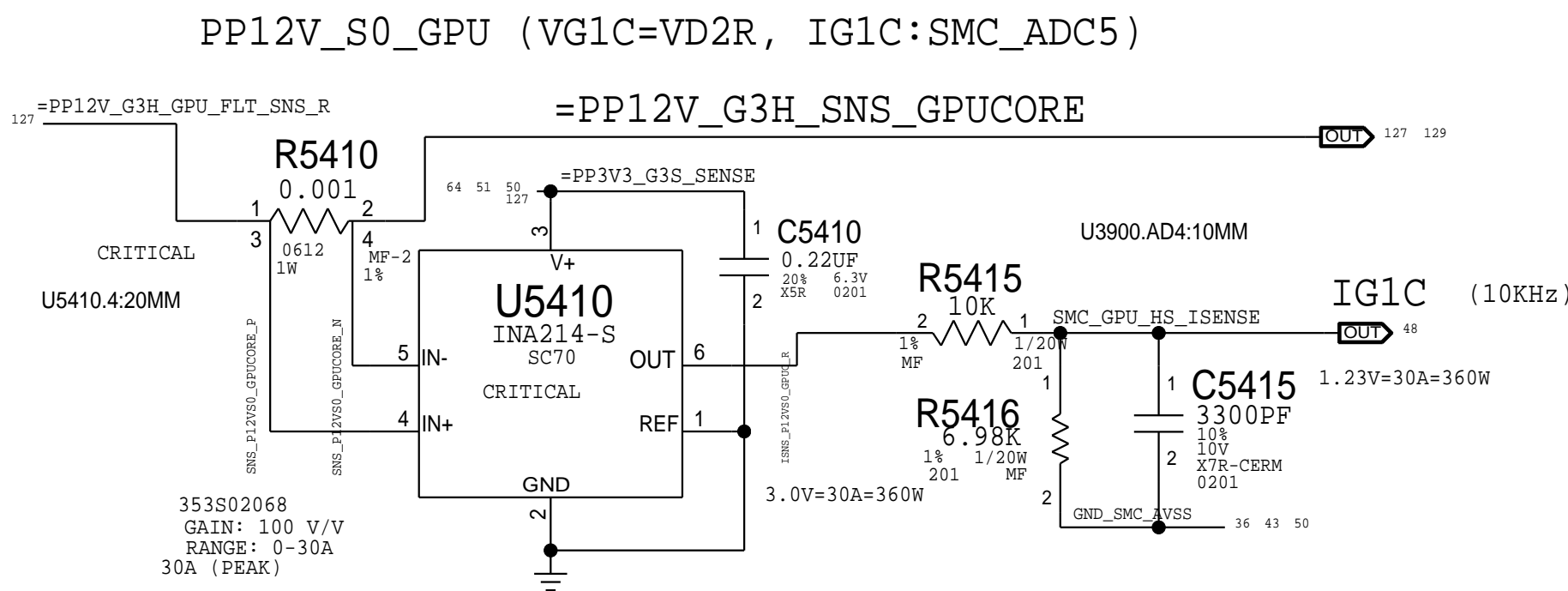
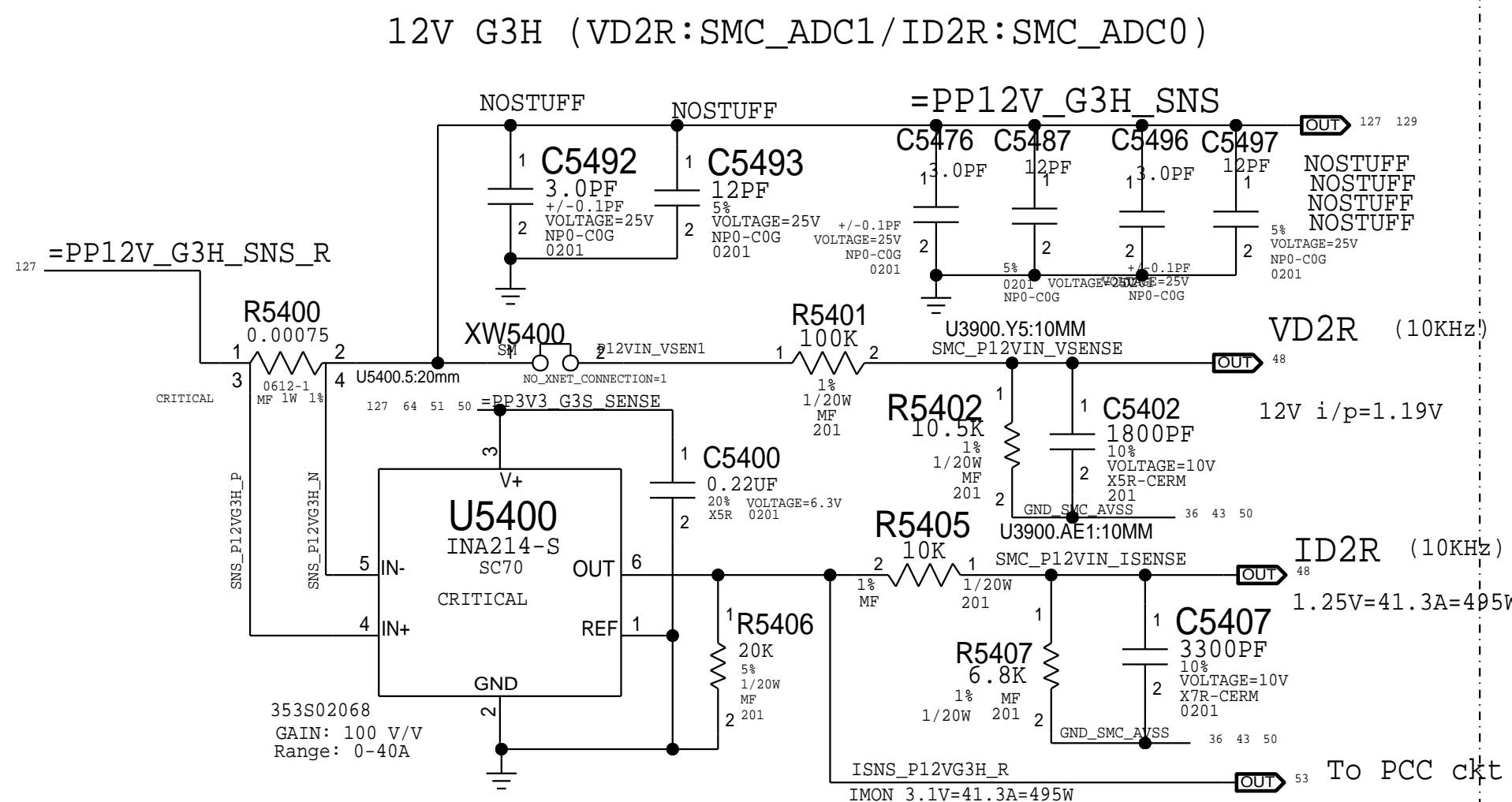


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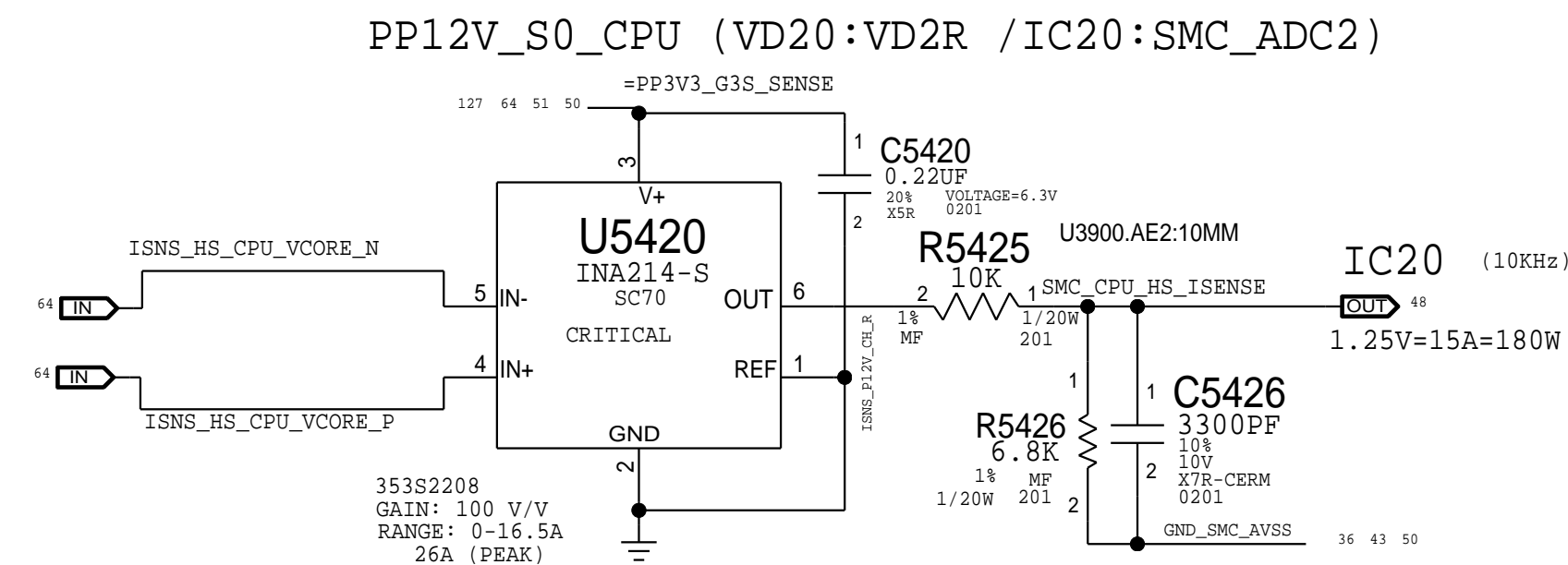
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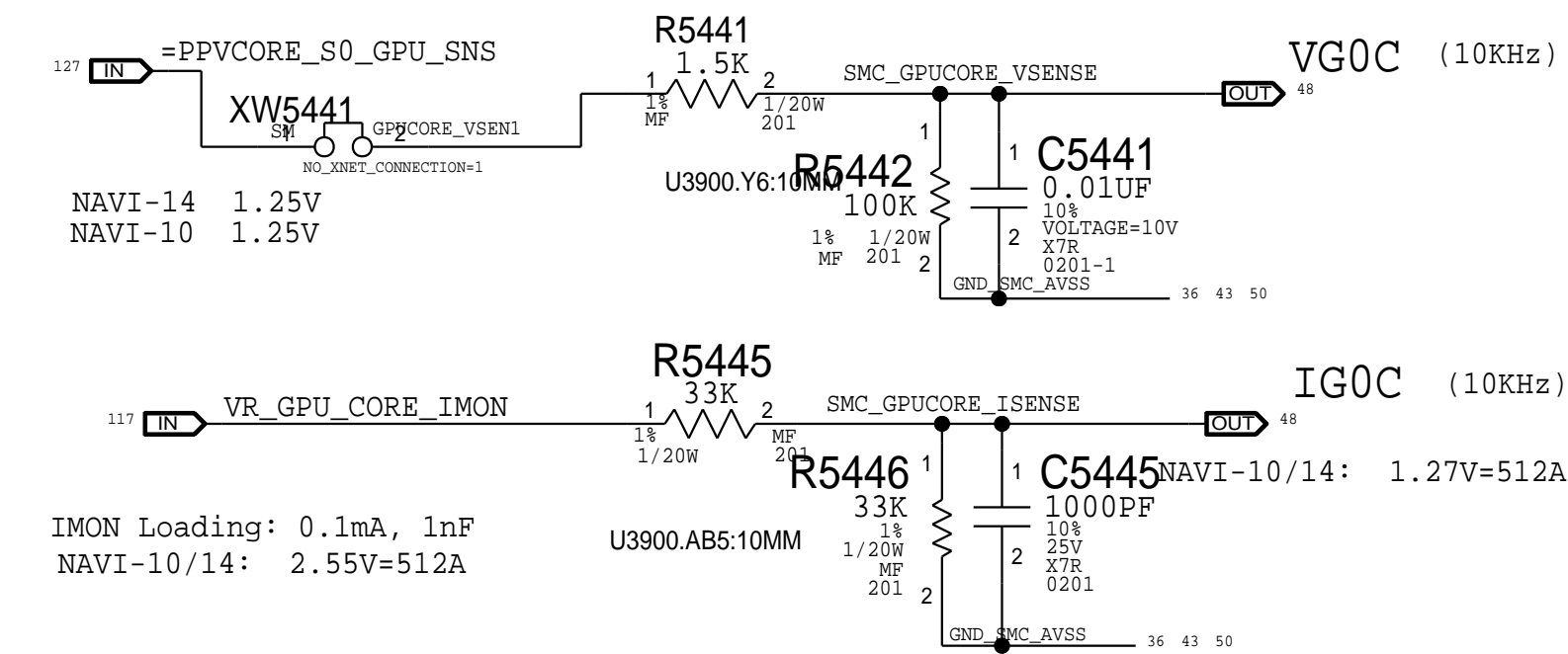


GPU AUX RAILS (VG1A=VD2R, IG1A:AMUX_A7) (100Hz)

GPU highside sense for GPU 0.9V & 1.8V VR

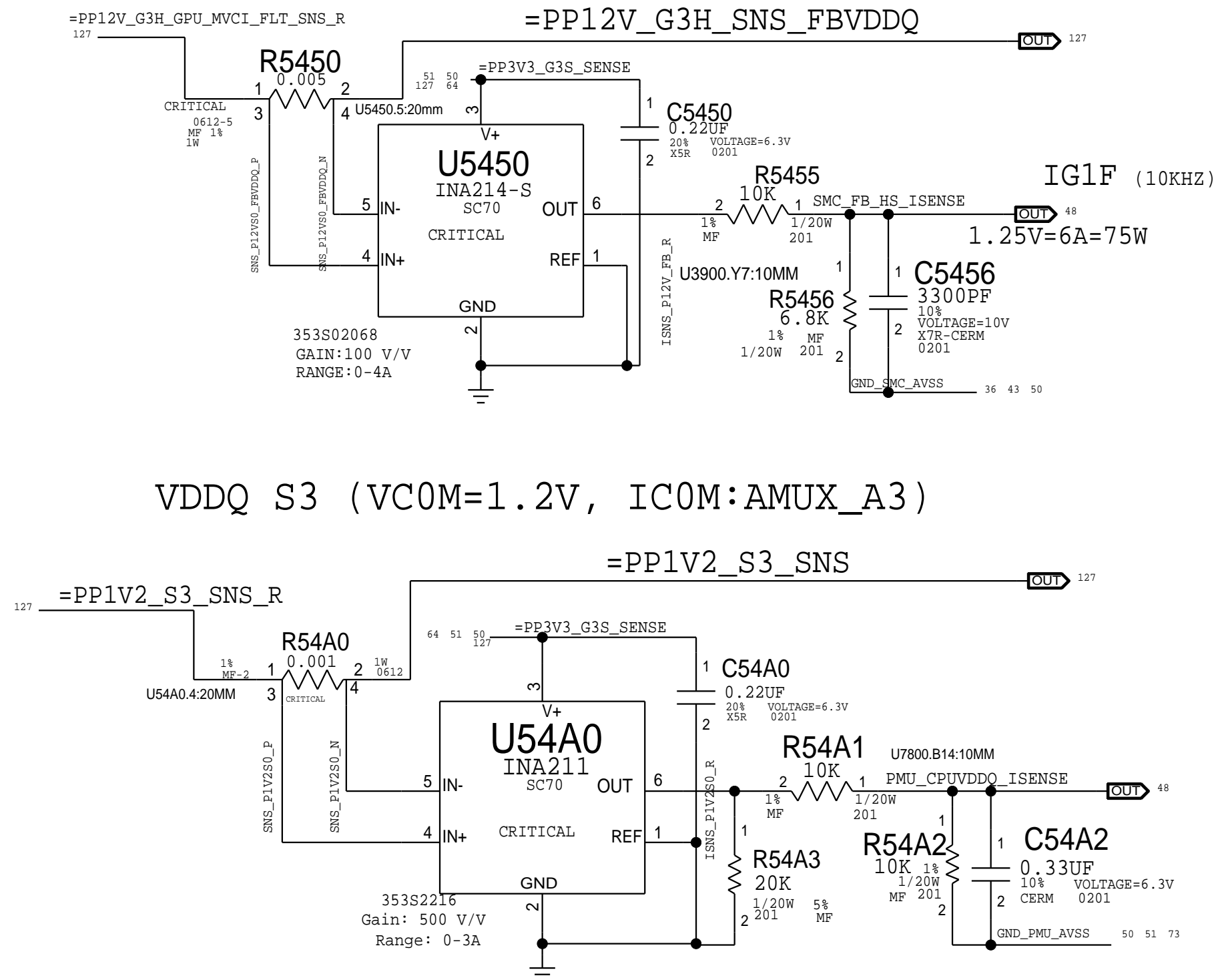


GPU CORE (VG0C:SMC_ADC7/IG0C:SMC_ADC3)

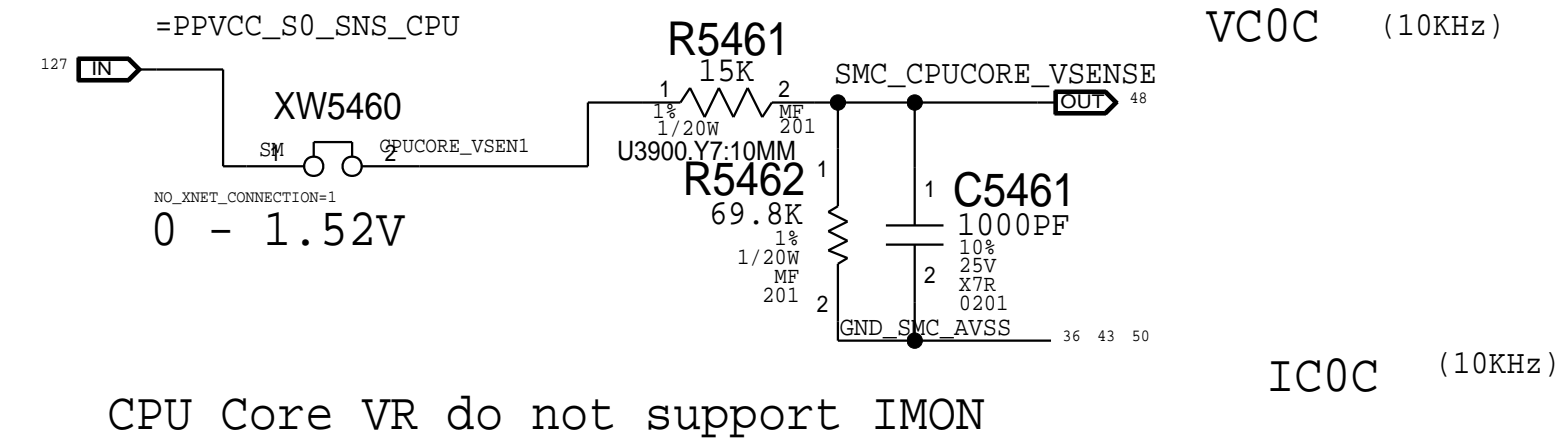


GPU FB (VG1F=VD20, IG1F:SMC_ADC4)

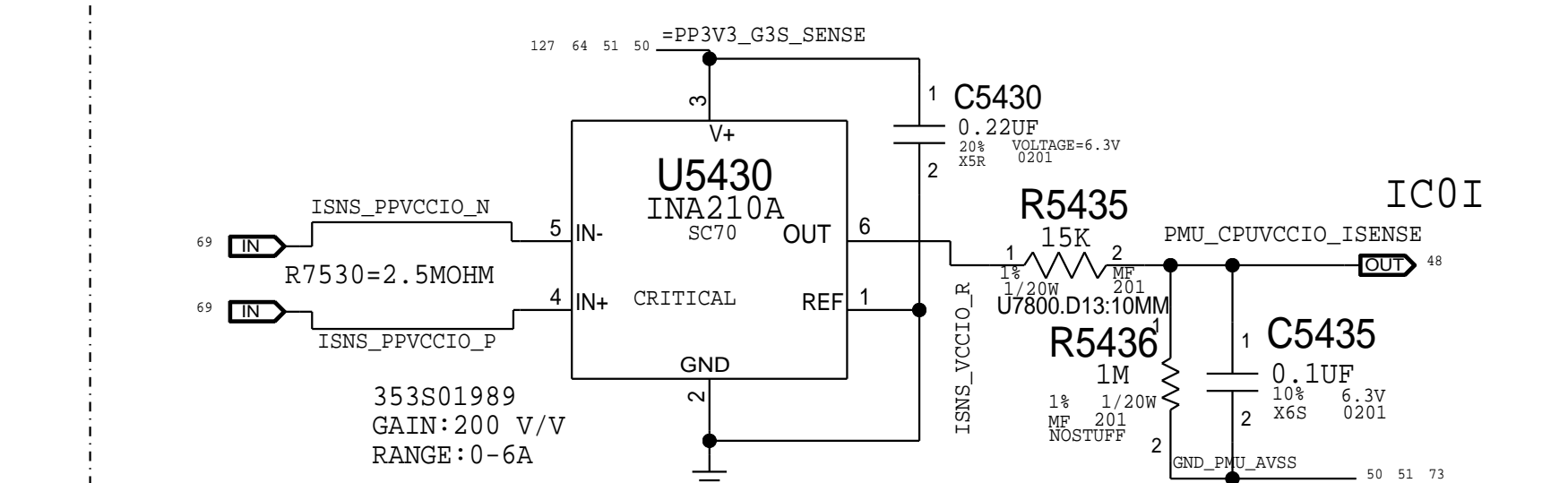
GPU highside sense for GPU FB 1.5V VDDQ VR



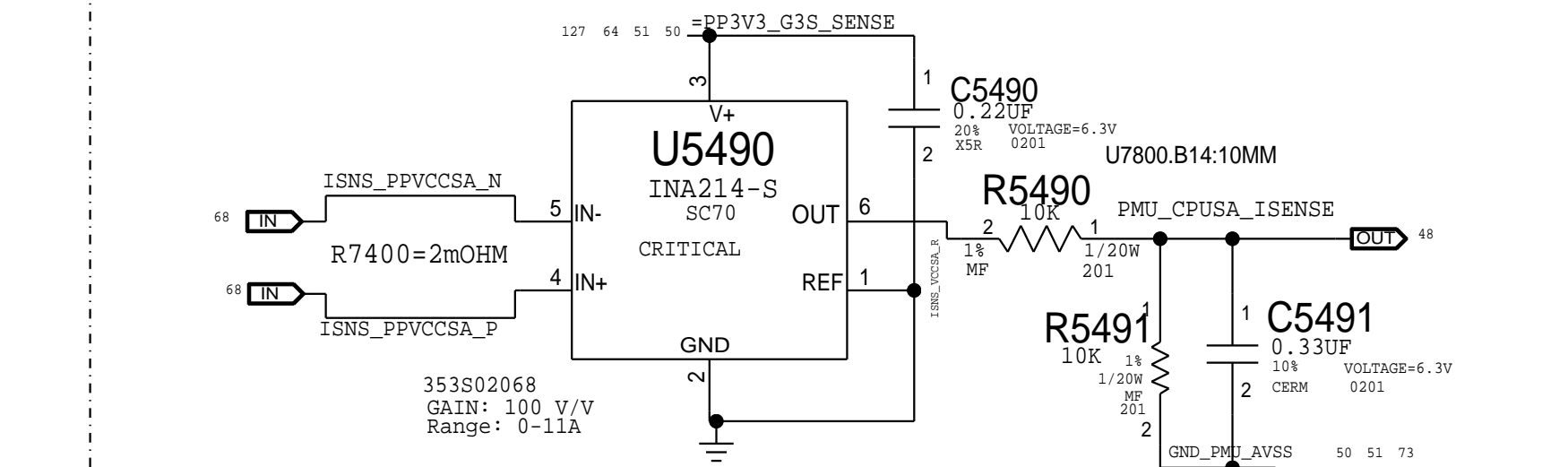
CPU CORE (VC0C:SMC_ADC6 /IC0C:NA)




CPU VCCIO (VC0I=0.95V, IC0I:AMUX_A0)



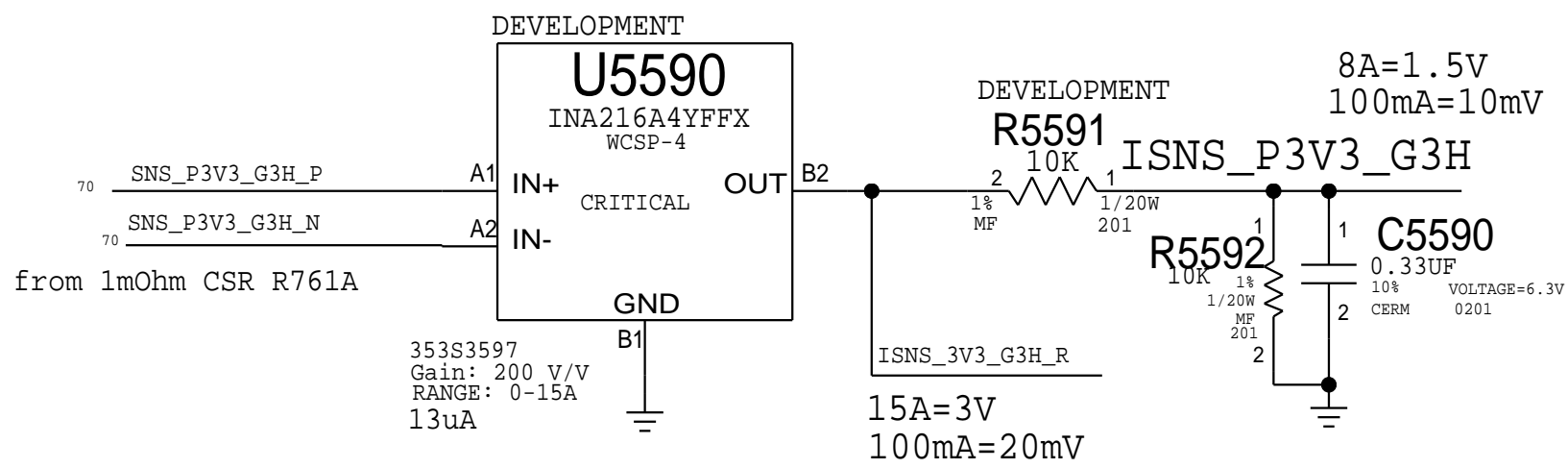
CPU CORE VCC_SA (VC0S=1.05V, IC0S:AMUX_A4)



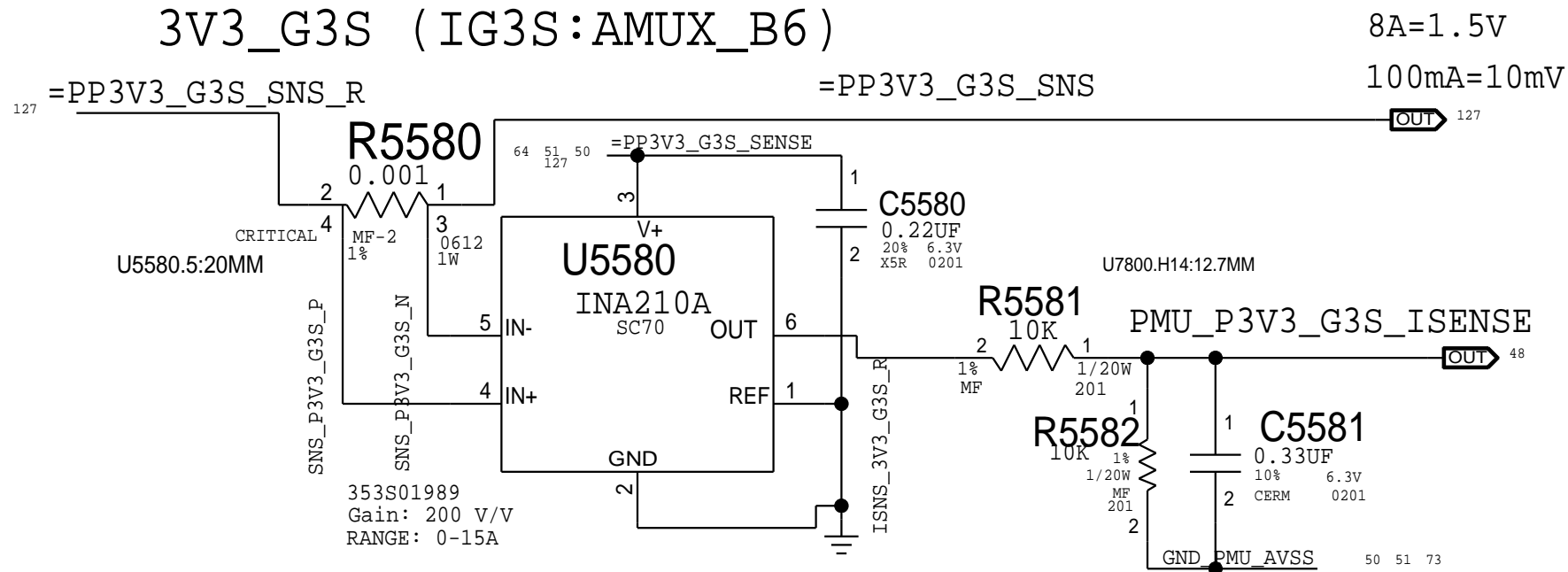
BOM_COST_GROUP=SENSORS

PAGE TITLE		
SENSORS: I and V Sense		
 Apple Inc.	DRAWING NUMBER	051-04705
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	PAGE	54 OF 172
	SHEET	50 OF 136

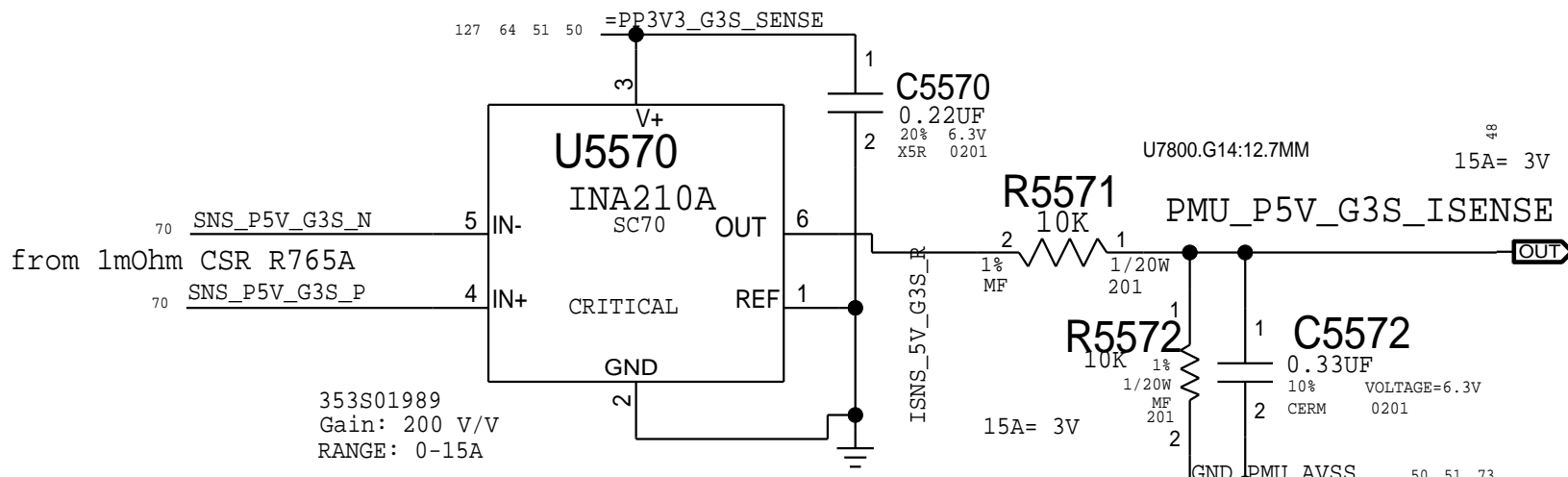
3V3_G3H MANUAL MEASUREMENT



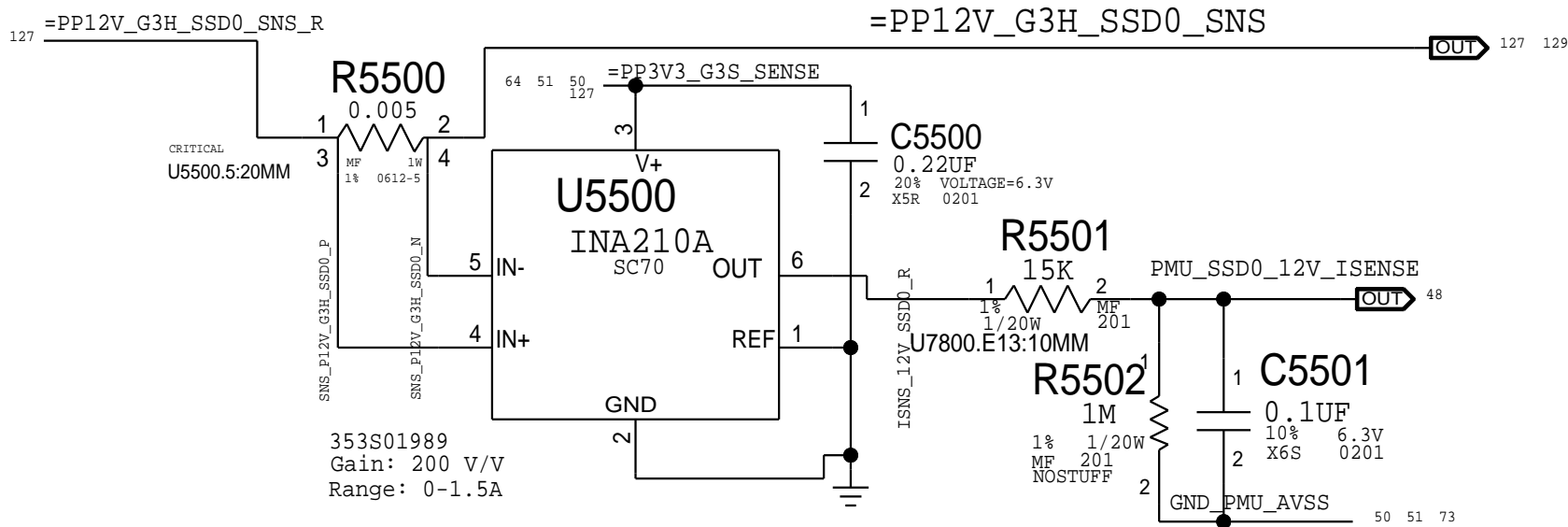
3V3_G3S (IG3S:AMUX_B6)



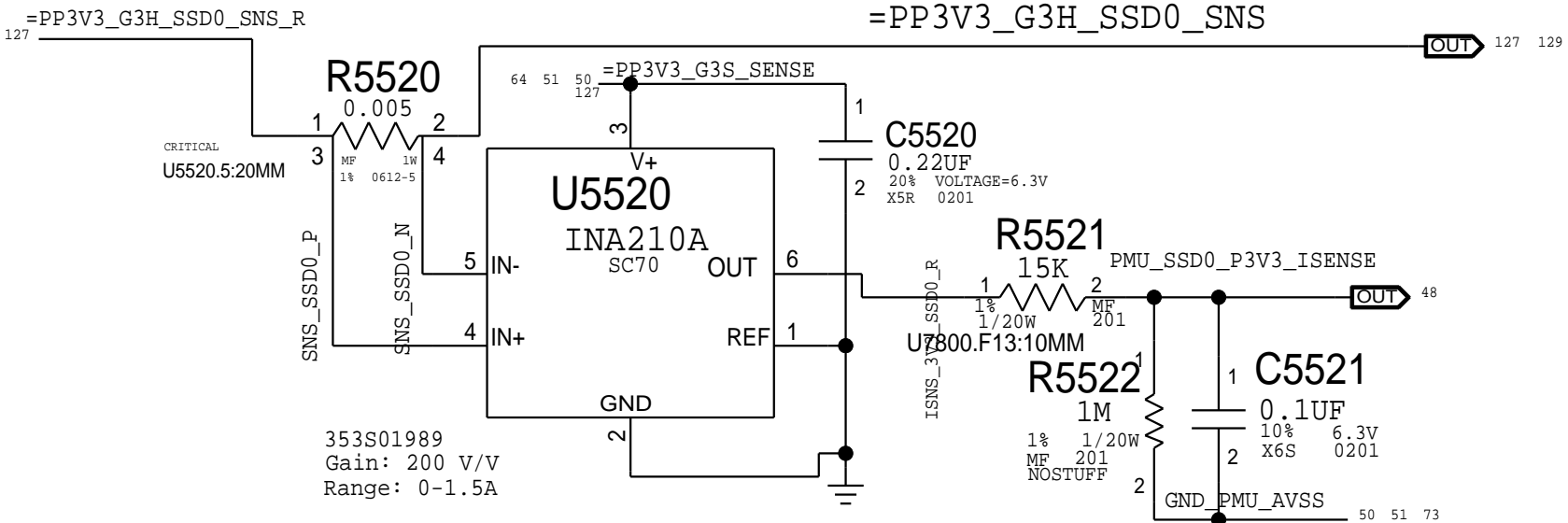
5V_G3S (IR45:AMUX_B5)



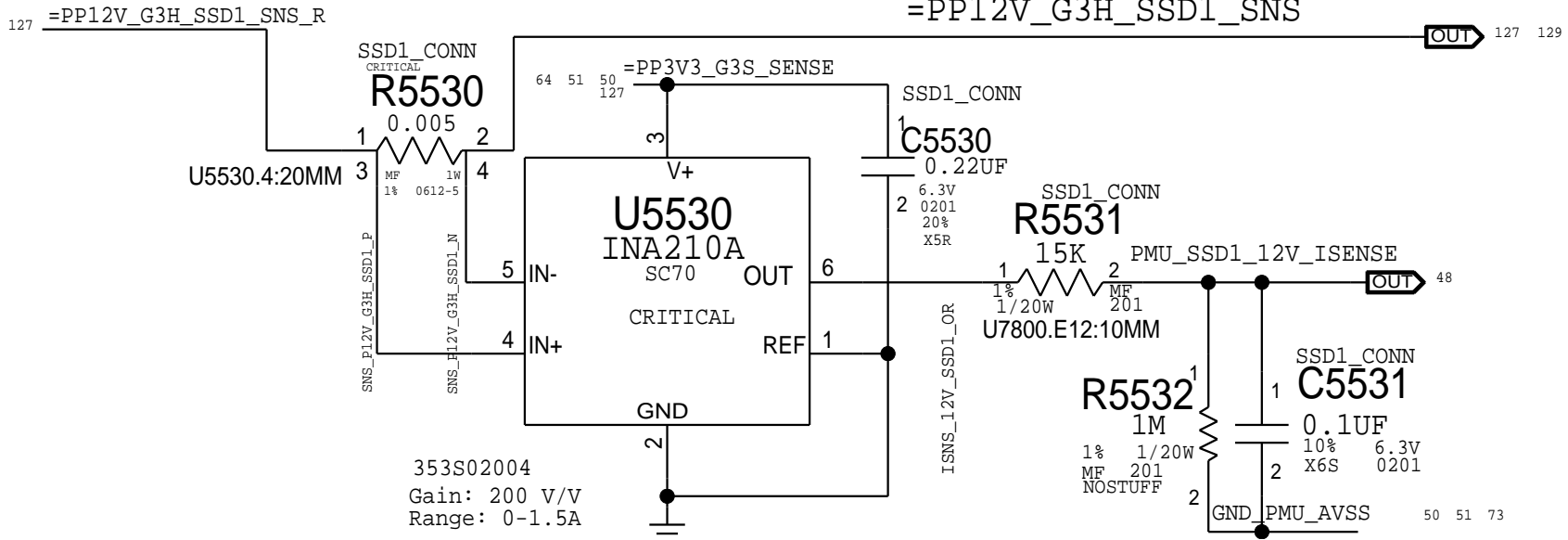
SSD0 PP12V_SSD0 (VH02:VD20/IH02:AMUX_B1)



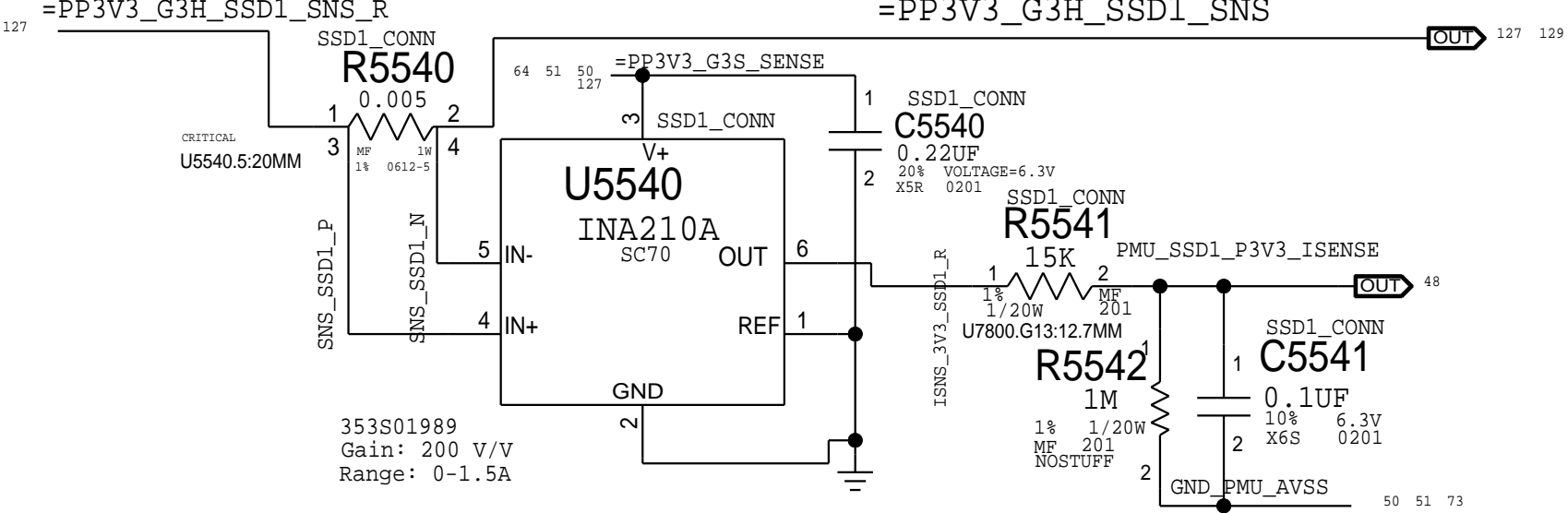
SSD0 (VR1R:3.3V/IH0R:AMUX_B3)



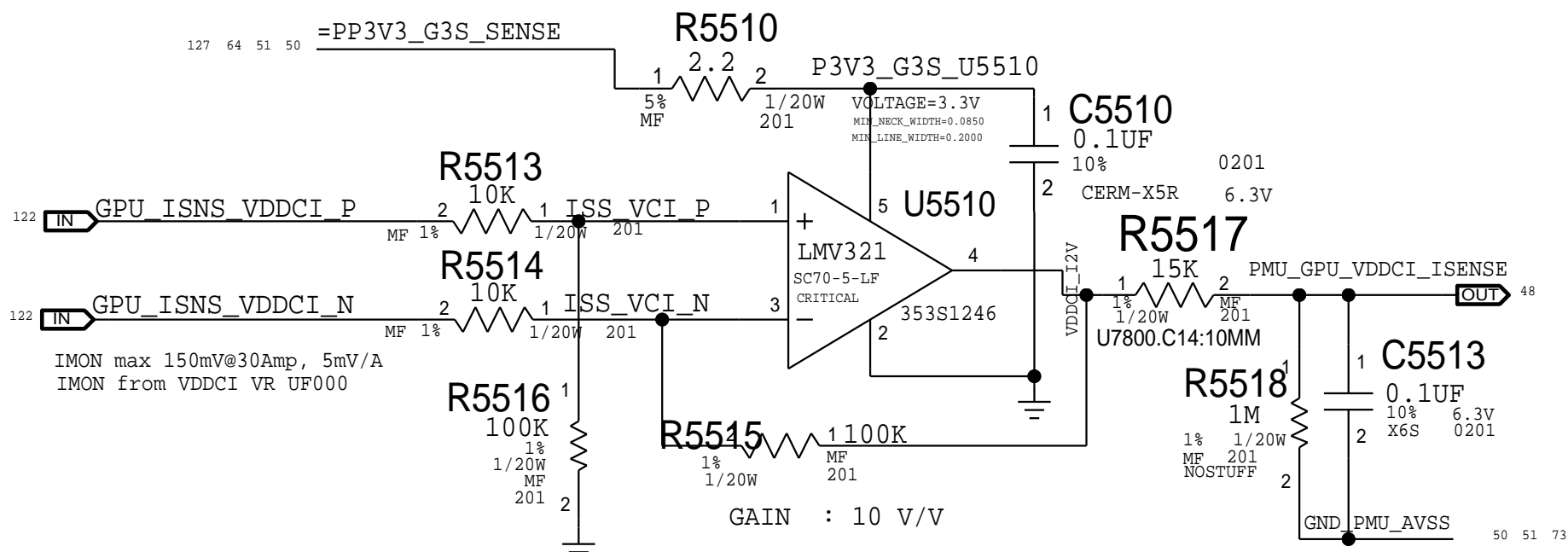
SSD1 PP12V_SSD1 (VH02:VD20/IH12:AMUX_B2)



SSD1 (VR1R:3.3V / IH1R:AMUX_B4)

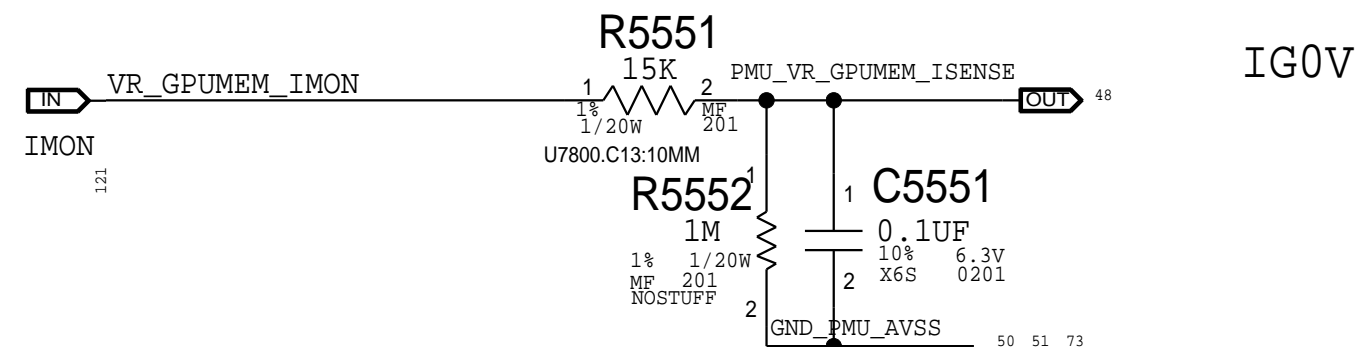


GPU_VDDCI S0 (VG0I:1V /IG0I: AMUX_A5)




Chip	Vref	Vmax	SMC_ADC_Freq	ADC_LPF
H9M	1.25V	1.8V	10Khz	10Khz
Calpe	1.5V	5V	100hz	100hz

GPU VDDIO/MVDD(VG0F:1.35V IG0F:AMUX_B0)



NAVI-10 1.5V=50A

BOM_COST_GROUP=SENSORS

PAGE TITLE		
SENSORS: I and V Sense(Continued)		
 Apple Inc.	DRAWING NUMBER	051-04705
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	PAGE	55 OF 172
	SHEET	51 OF 136

D

C

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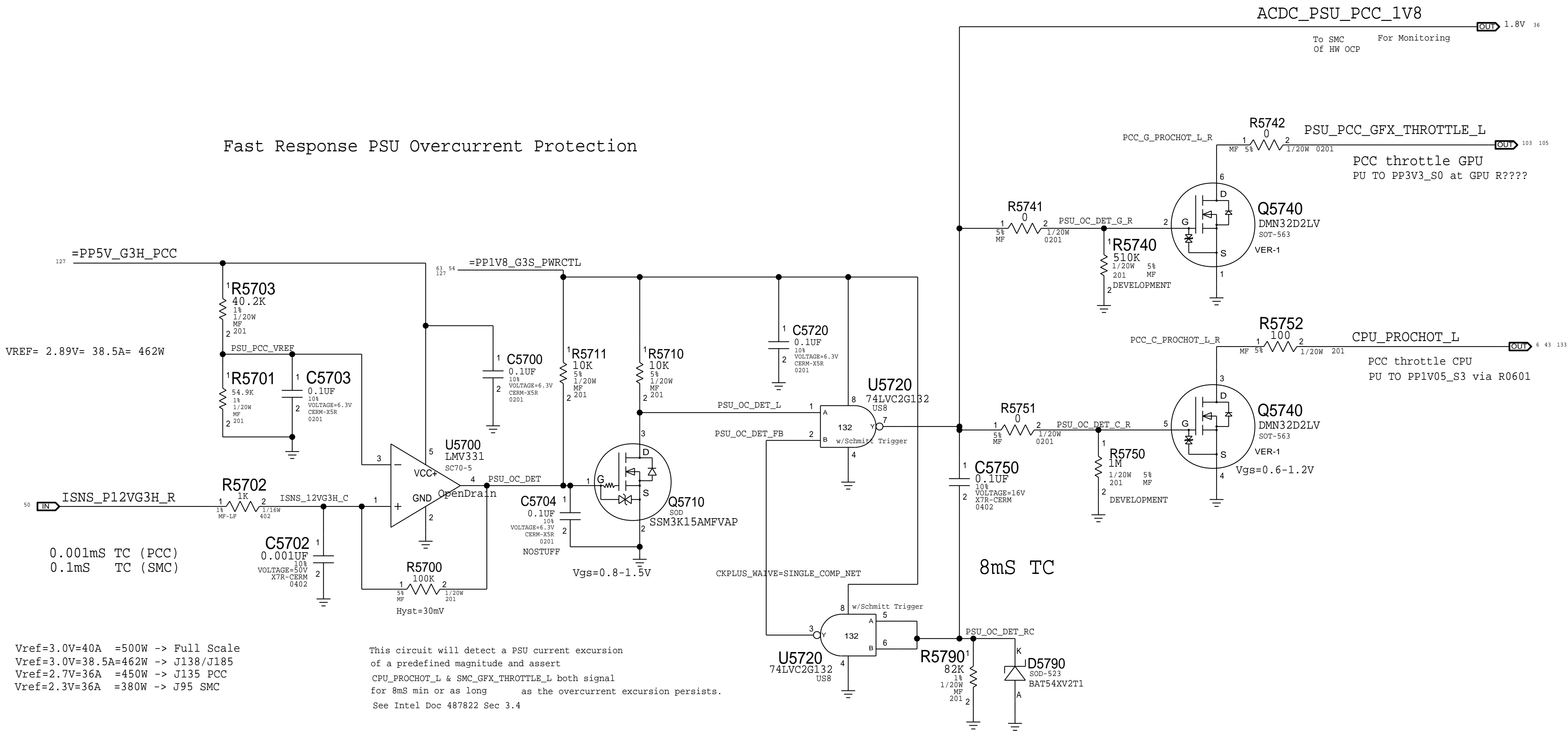
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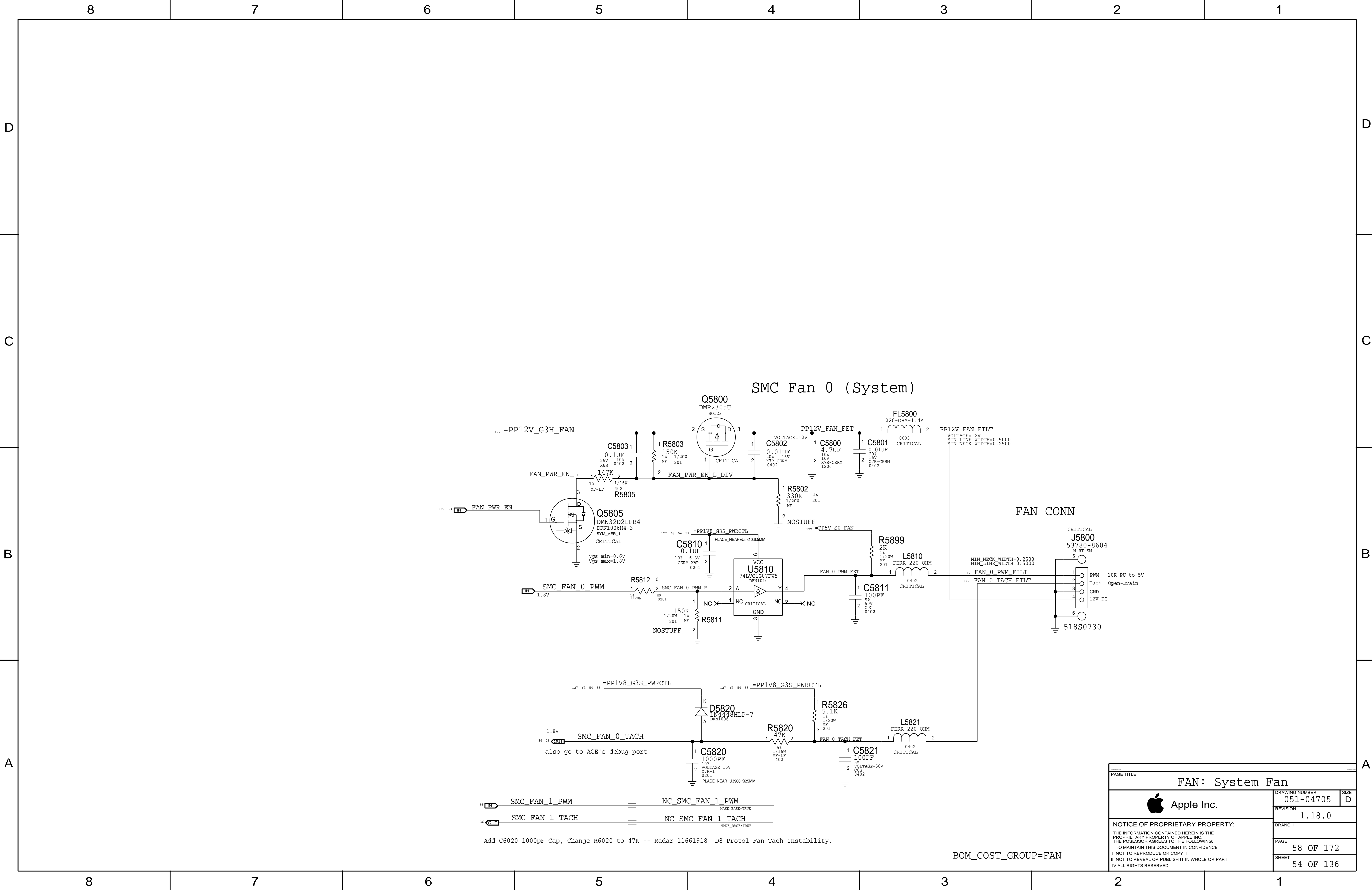
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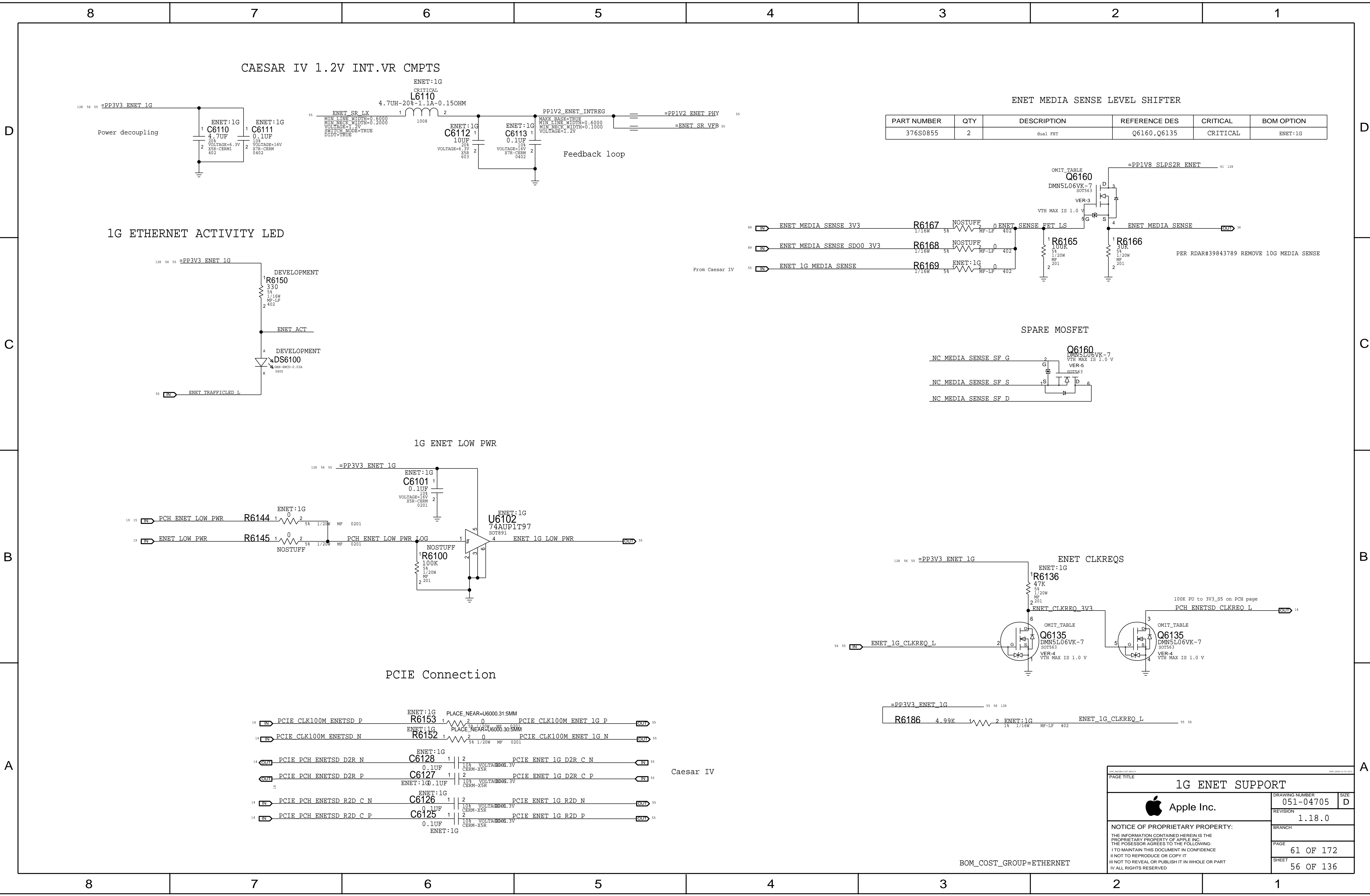
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PAGE TITLE		
SENSORS: PSU/PCC		
 Apple Inc.	DRAWING NUMBER	051-04705
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1G ETHERNET ACTIVITY LED

1285655=PP3V3_ENET_1G

DEVELOPMENT

R6150

330

5%

1/16W

MF-LF

402

ENET_ACT

DEVELOPMENT

DS6100

0805

DRN-SMD-0.03A

ENET_TRAFFICLED_L

1G ENET LOW PWR

1285655=PP3V3_ENET_1G

ENET:1G

C6101

0.1UF

VOLTAGE=16V

X5R-CERM

0201

PCH_ENET_LOW_PWR

R6144

0

5%

1/20W

MF

0201

ENET:1G

R6145

0

5%

1/20W

MF

0201

ENET_LOW_PWR

PCH_ENET_LOW_PWR

LOG

NOSTUFF

R6100

100K

5%

1/20W

MF

201

ENET:1G

U6102

74AUP1T97

SOT891

ENET_1G_LOW_PWR

PCIE Connection

PCIE_CLK100M_ENETSD_P

R6153

0

PLACE_NEAR=U6000.31:5MM

PCIE_CLK100M_ENET_1G_P

PCIE_CLK100M_ENETSD_N

R6152

0

PLACE_NEAR=U6000.30:5MM

PCIE_CLK100M_ENET_1G_N

PCIE_PCH_ENETSD_D2R_N

C6128

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_D2R_C_N

PCIE_PCH_ENETSD_D2R_P

C6127

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_D2R_C_P

PCIE_PCH_ENETSD_R2D_C_N

C6126

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_R2D_N

PCIE_PCH_ENETSD_R2D_C_P

C6125

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_R2D_P

ENET MEDIA SENSE LEVEL SHIFTER

PART NUMBER

QTY

DESCRIPTION

REFERENCE DES

CRITICAL

BOM OPTION

376S0855

2

dual FET

Q6160,Q6135

CRITICAL

ENET:1G

ENET MEDIA SENSE 3V3

R6167

NOSTUFF

1/16W

5%

MF-LF

402

ENET MEDIA SENSE SDO0 3V3

R6168

NOSTUFF

1/16W

5%

MF-LF

402

ENET_1G_MEDIA_SENSE

R6169

ENET:1G

1/16W

5%

MF-LF

402

SENSE

FET_LS

R6165

100K

5%

1/20W

MF

201

Q6160

DMN5L06VK-7

SOT563

VER-3

VTH_MAX_IS_1.0_V

ENET_MEDIA_SENSE

SPARE MOSFET

NC_MEDIA_SENSE_SF_G

NC_MEDIA_SENSE_SF_S

NC_MEDIA_SENSE_SF_D

Q6160

DMN5L06VK-7

SOT563

VER-5

VTH_MAX_IS_1.0_V

ENET CLKREQS

1285655=PP3V3_ENET_1G

ENET:1G

R6136

47K

5%

1/20W

MF

201

ENET_CLKREQ_3V3

Q6135

DMN5L06VK-7

SOT563

VER-4

VTH_MAX_IS_1.0_V

ENET_1G_CLKREQ_L

Q6135

DMN5L06VK-7

SOT563

VER-4

VTH_MAX_IS_1.0_V

100K_PU_to_3v3_S5_on_PCH_page

PCH_ENETSD_CLKREQ_L

=PP3V3_ENET_1G

R6186

4.99K

1%

1/16W

MF-LF

402

ENET_1G_CLKREQ_L

Caesar IV

PCIE_CLK100M_ENETSD_P

R6153

0

PLACE_NEAR=U6000.31:5MM

PCIE_CLK100M_ENET_1G_P

PCIE_CLK100M_ENETSD_N

R6152

0

PLACE_NEAR=U6000.30:5MM

PCIE_CLK100M_ENET_1G_N

PCIE_PCH_ENETSD_D2R_N

C6128

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_D2R_C_N

PCIE_PCH_ENETSD_D2R_P

C6127

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_D2R_C_P

PCIE_PCH_ENETSD_R2D_C_N

C6126

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_R2D_N

PCIE_PCH_ENETSD_R2D_C_P

C6125

0.1UF

10% VOLTAGE=6.3V

CERM-X5R

PCIE_ENET_1G_R2D_P

BOM_COST_GROUP=ETHERNET

1G ENET SUPPORT

Apple Inc.

051-04705

1.18.0

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A

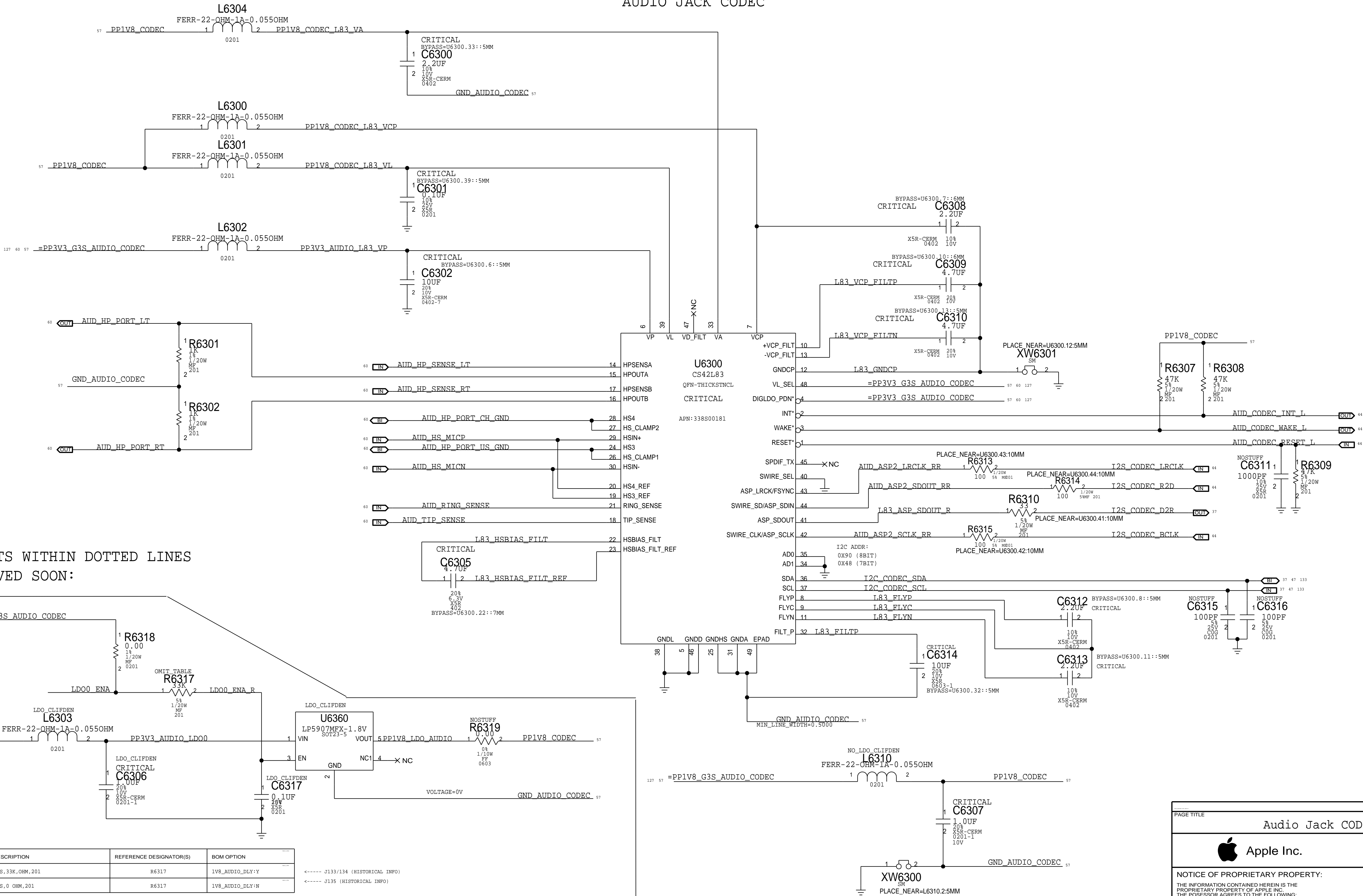
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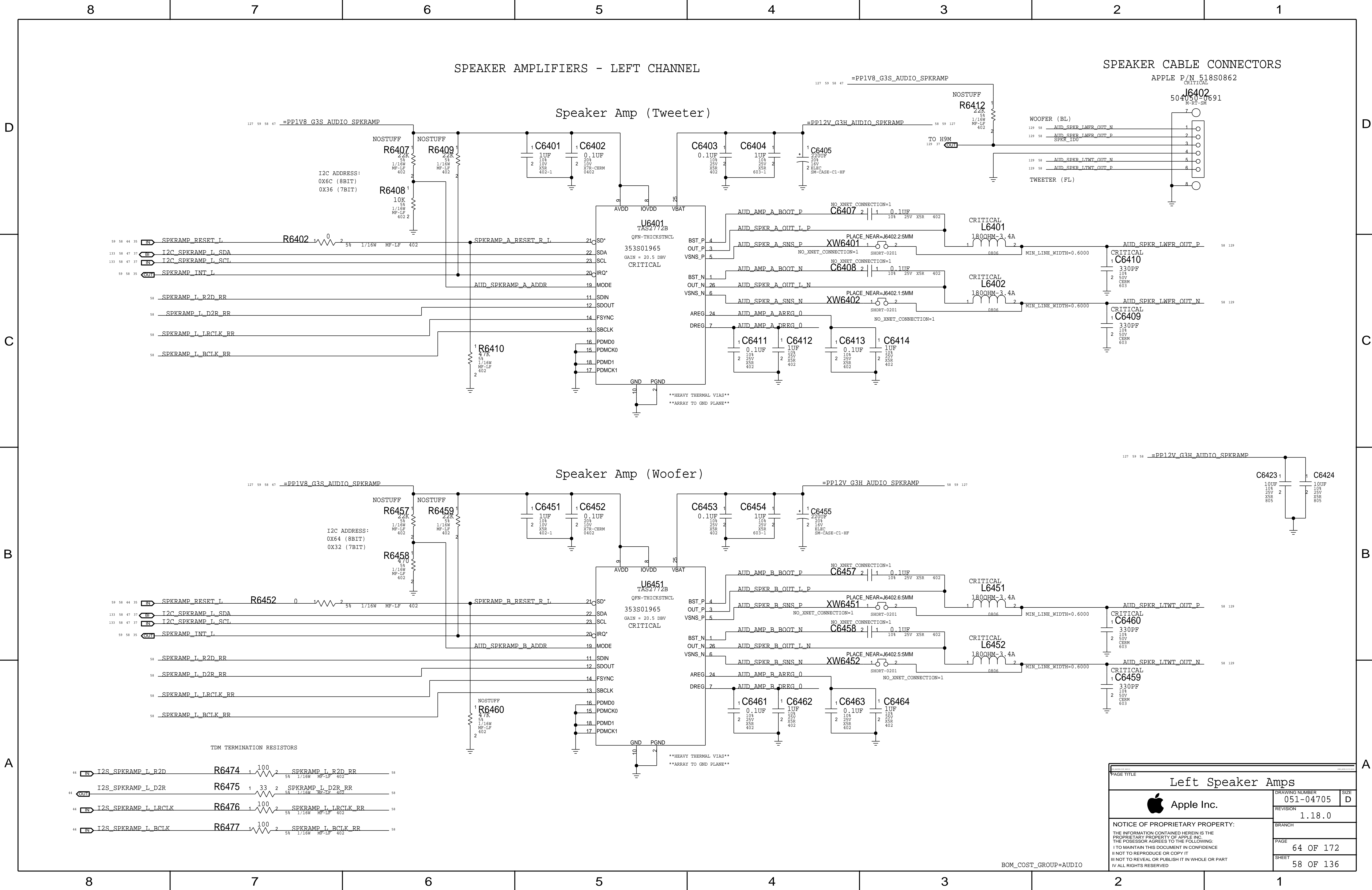
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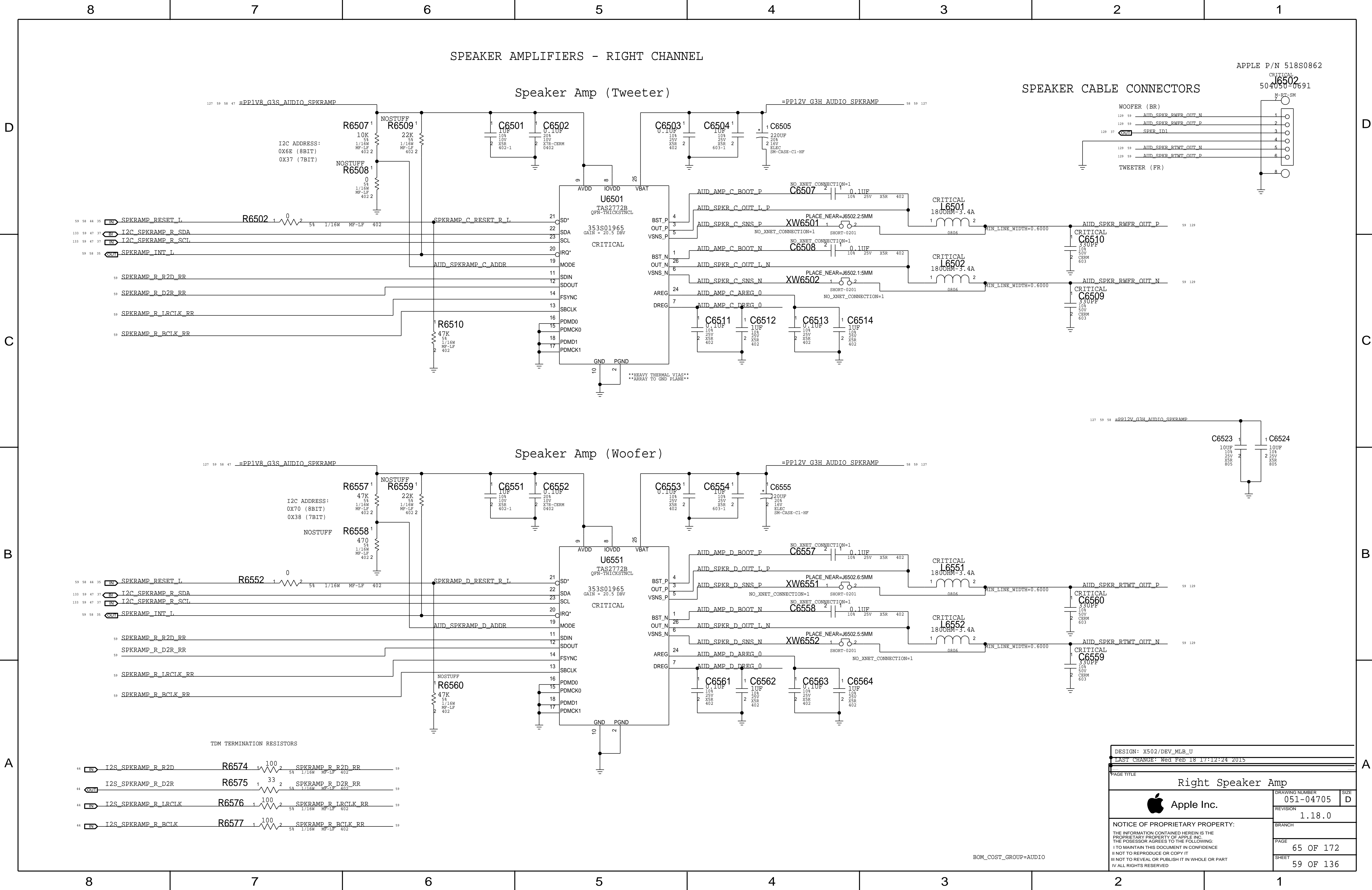
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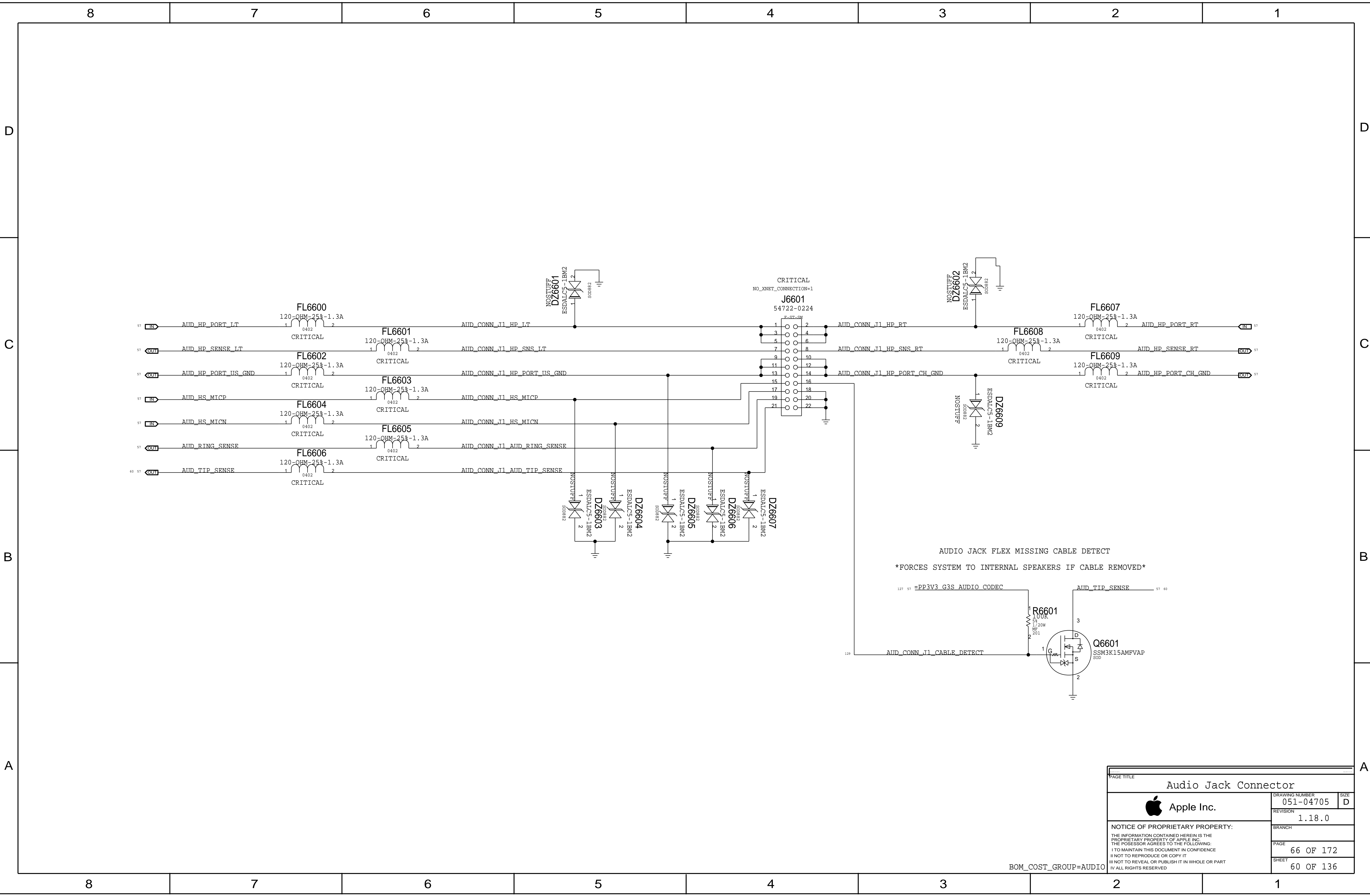
AUDIO JACK CODEC




BOM_COST_GROUP=AUDIO

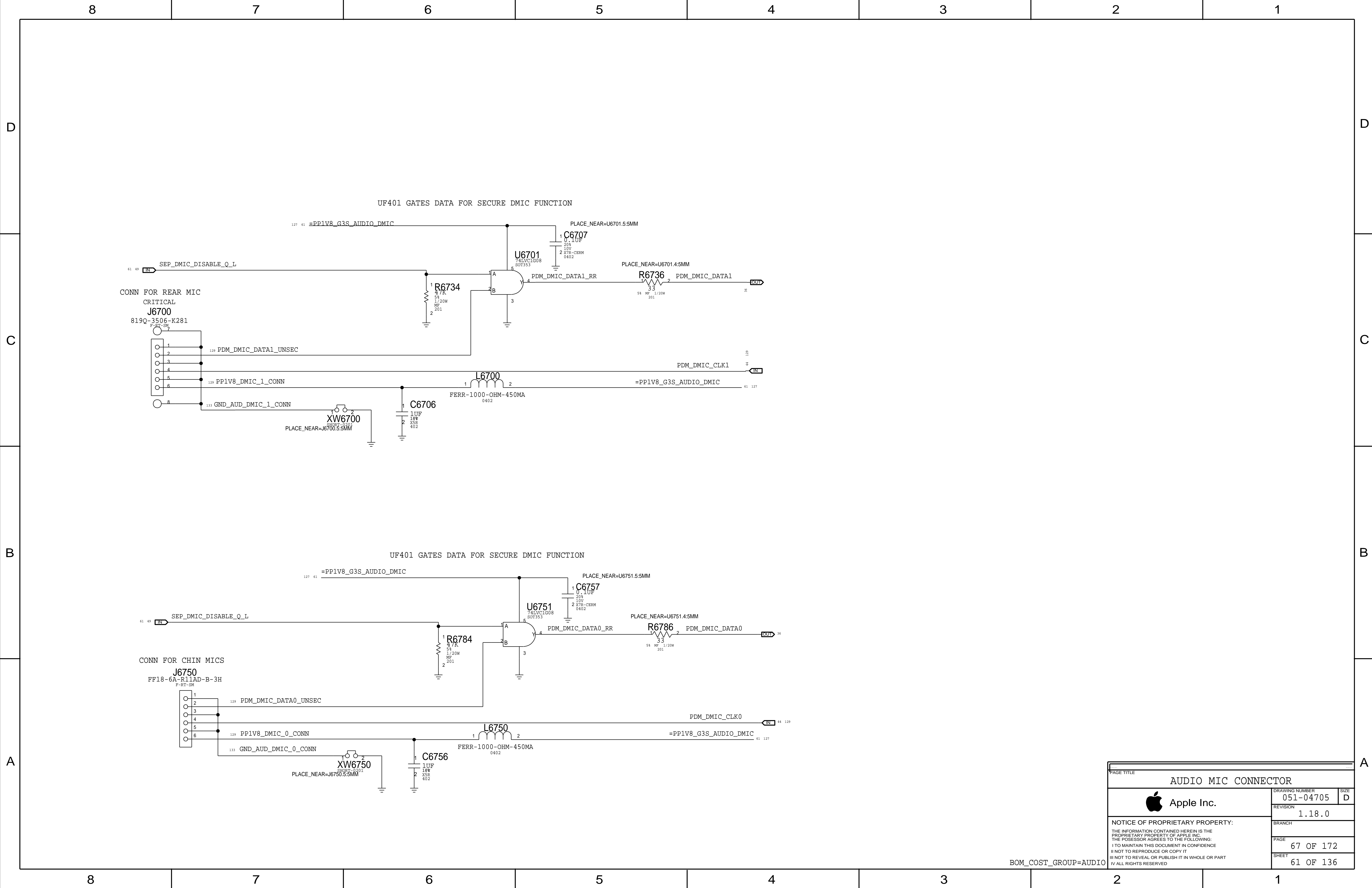





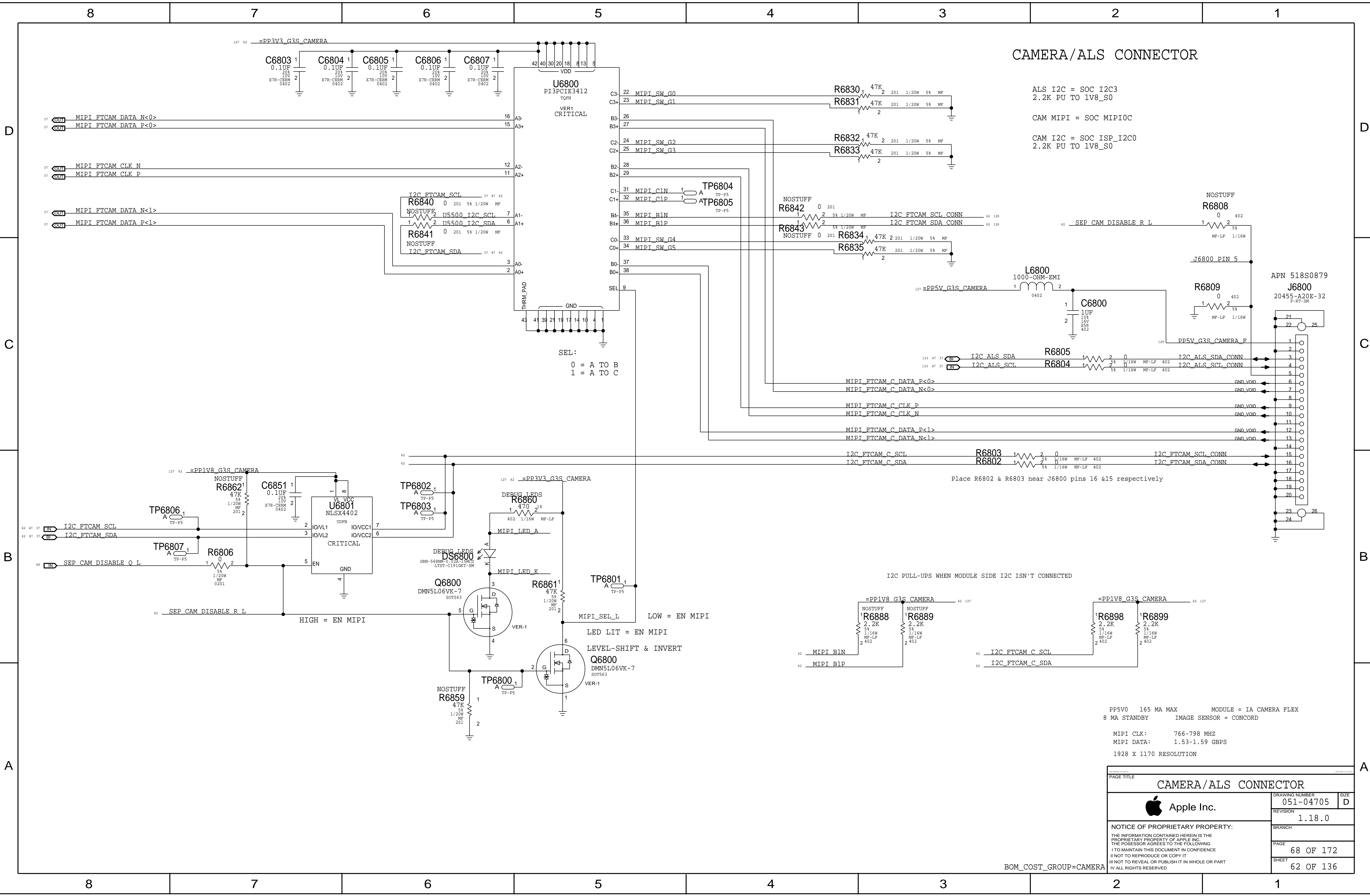


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Audio Jack Connector		
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BOM_COST_GROUP=AUDIO



PAGE TITLE		
AUDIO MIC CONNECTOR		
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	SHEET	61 OF 136



CAMERA/ALS CONNECTOR

ALS I2C = SOC I2C3
2.2K PU TO 1V8_S0

CAM MIPI = SOC MIPI0C

CAM I2C = SOC ISP_I2C0
2.2K PU TO 1V8_S0

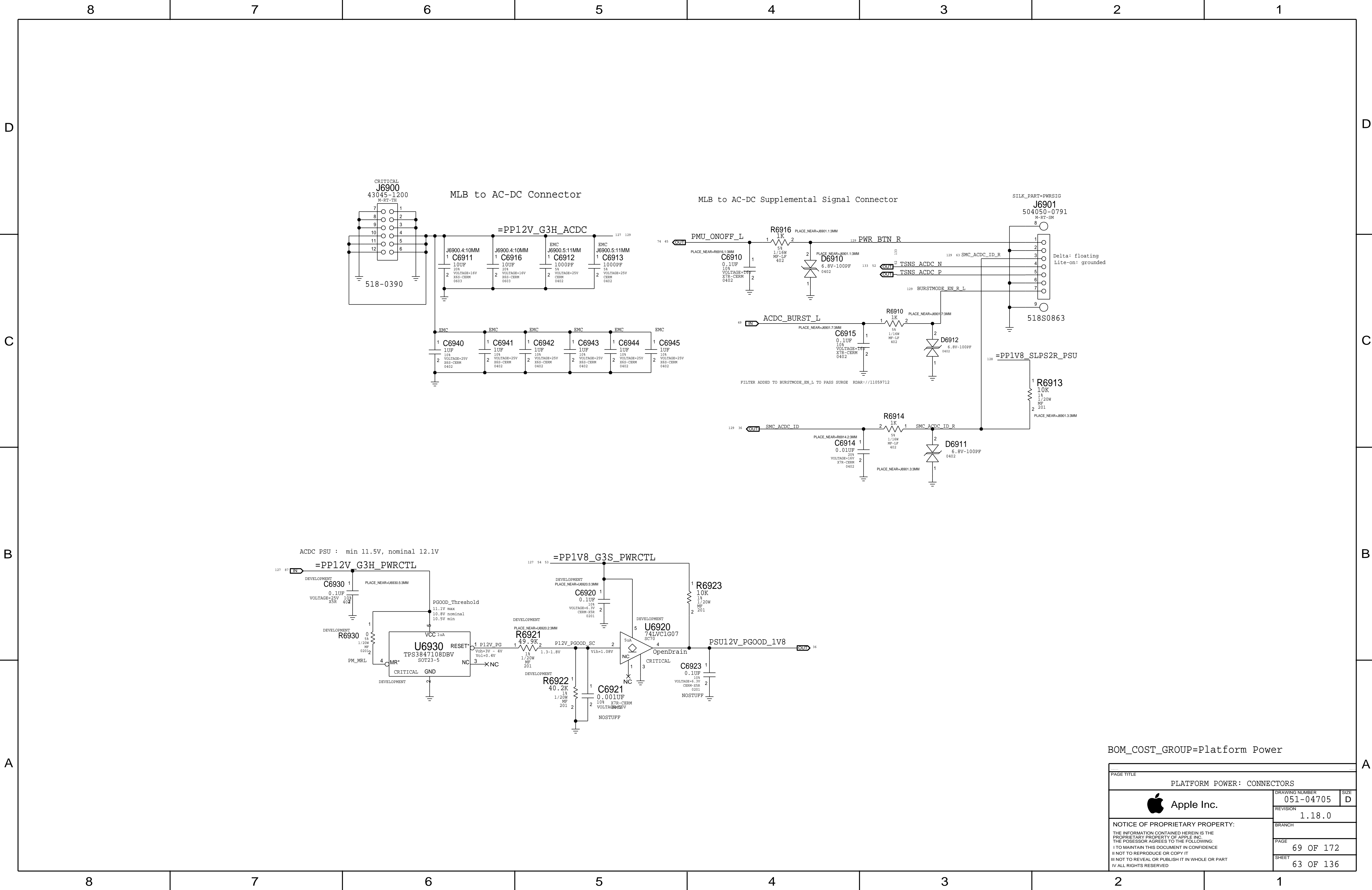
PP5V0 165 MA MAX MODULE = IA CAMERA FLEX
8 MA STANDBY IMAGE SENSOR = CONCORD

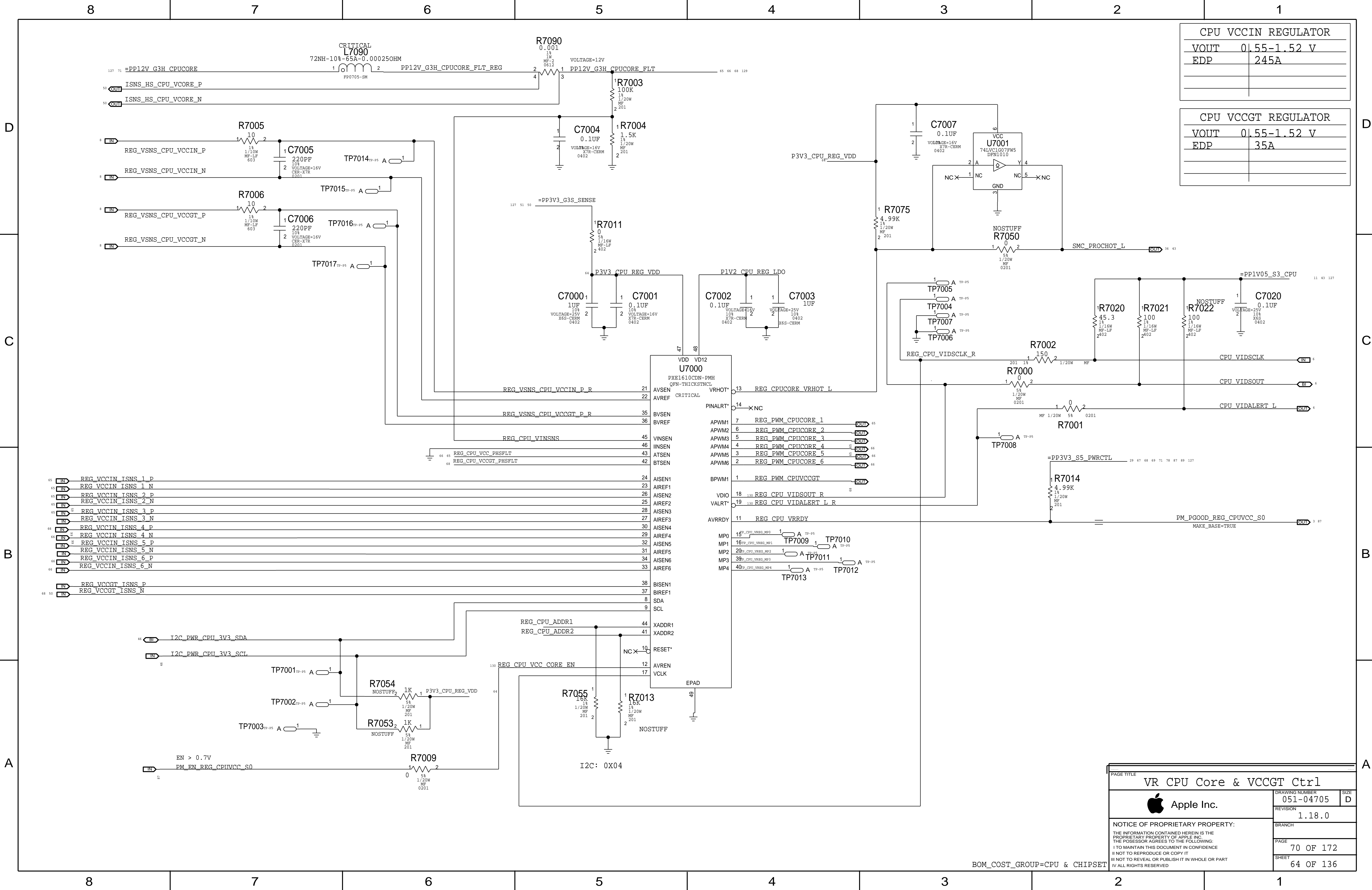
MIPI CLK: 766-798 MHZ
MIPI DATA: 1.53-1.59 GBPS

1928 X 1170 RESOLUTION

PAGE TITLE		
CAMERA/ALS CONNECTOR		
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BOM_COST_GROUP=CAMERA

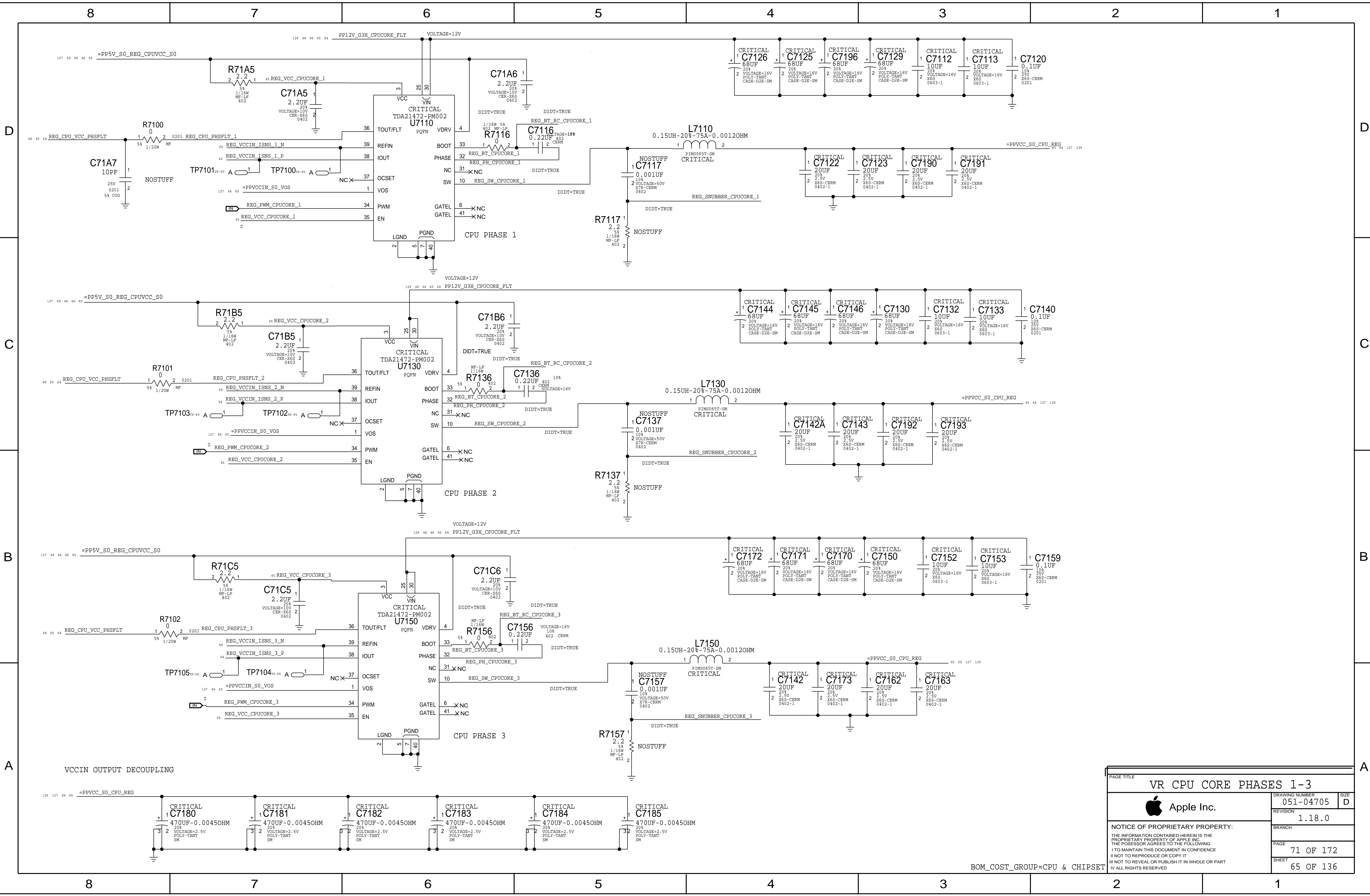





CPU VCCIN REGULATOR	
VOUT	0.55-1.52 V
EDP	245A

CPU VCCGT REGULATOR	
VOUT	0.55-1.52 V
EDP	35A

PAGE TITLE		
VR CPU Core & VCCGT Ctrl		
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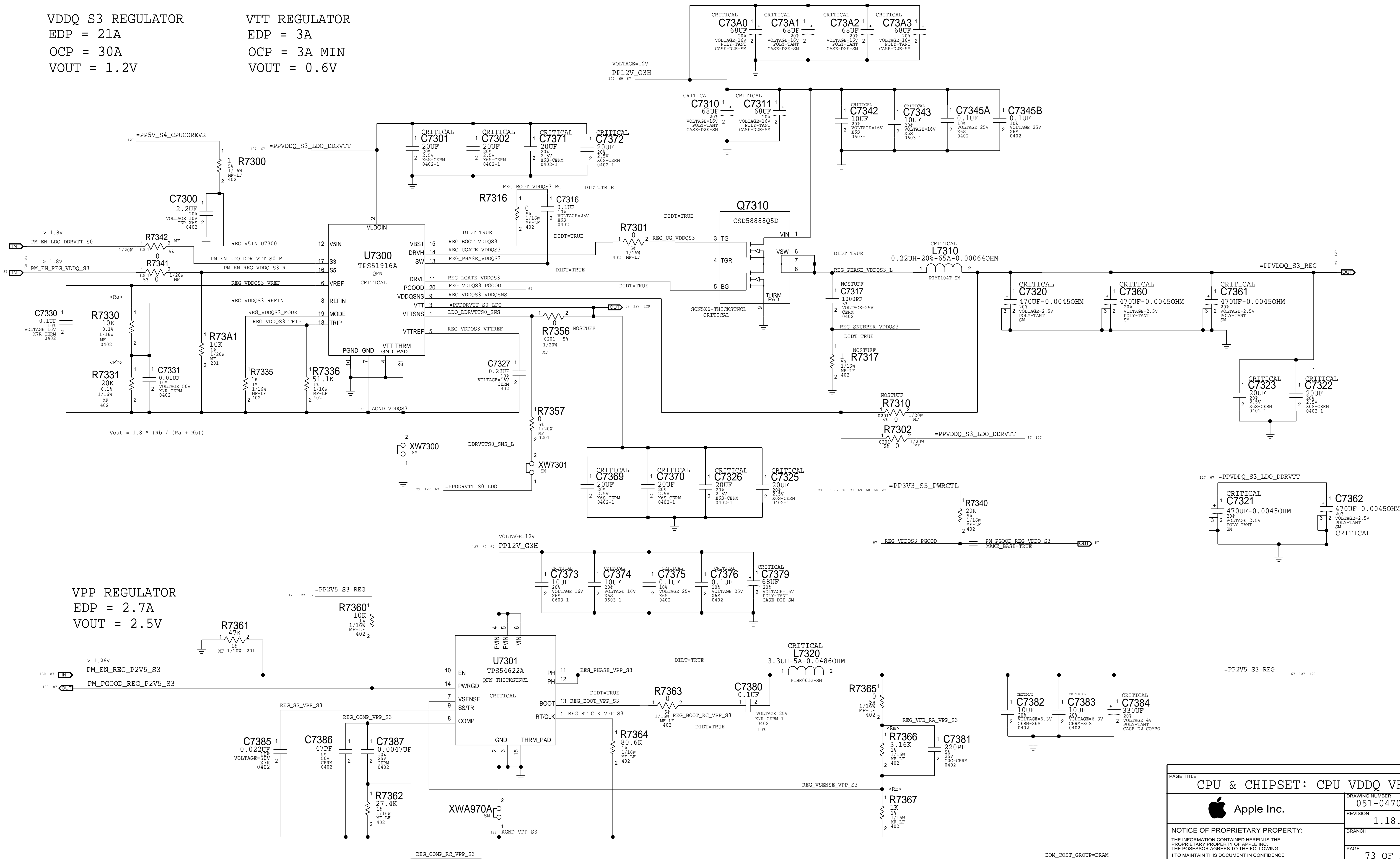
PAGE TITLE		
VR CPU CORE PHASES 1-3		
 Apple Inc.	DRAWING NUMBER	051-04705
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BOM_COST_GROUP=CPU & CHIPSET

VDDQ S3 REGULATOR
EDP = 21A
OCP = 30A
VOUT = 1.2V

VTT REGULATOR
EDP = 3A
OCP = 3A MIN
VOUT = 0.6V

VPP REGULATOR
EDP = 2.7A
VOUT = 2.5V



PAGE TITLE		
CPU & CHIPSET: CPU VDDQ VR		
 Apple Inc.	DRAWING NUMBER	051-04705
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	PAGE	73 OF 172
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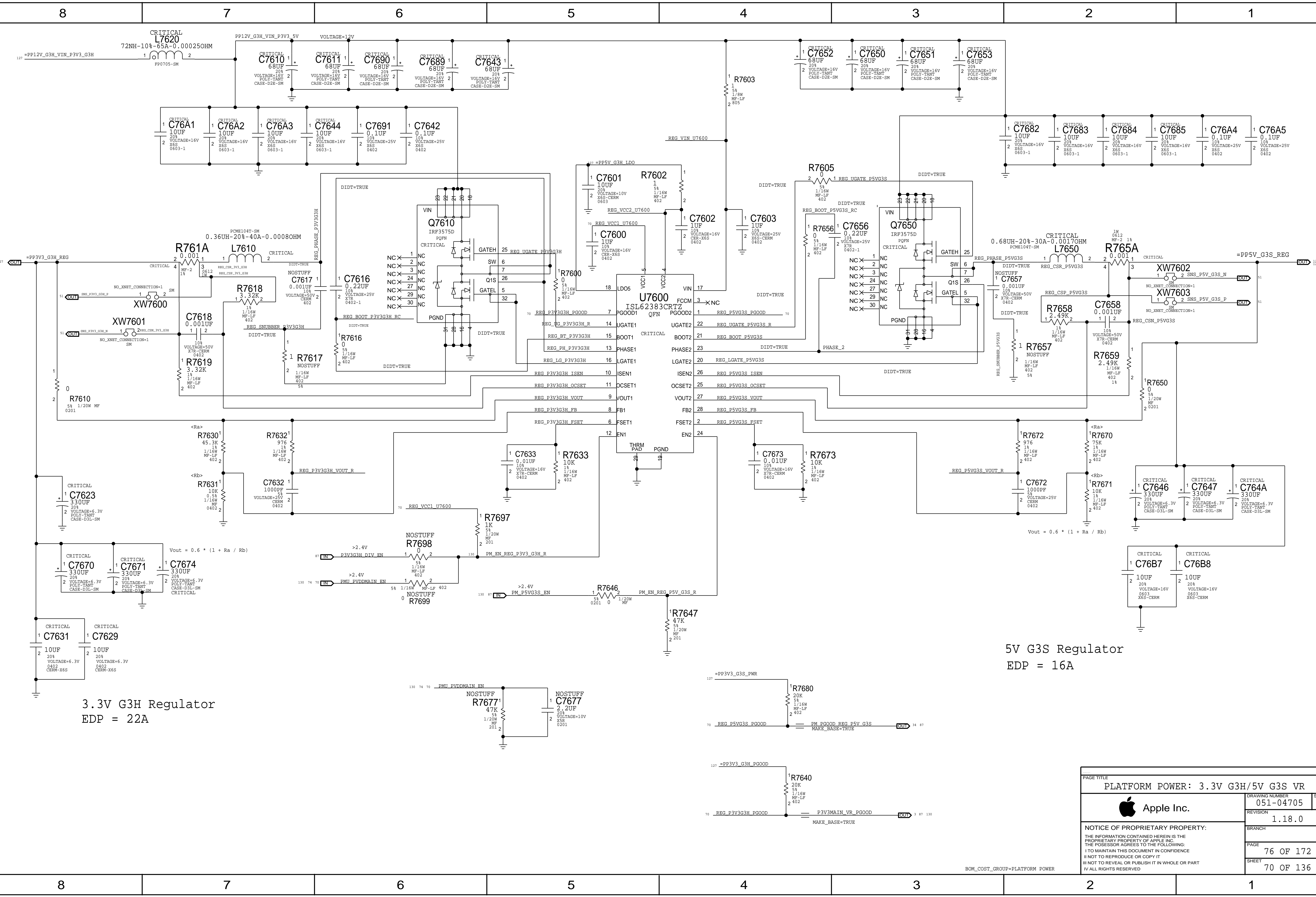
A

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B

A



5V G3S Regulator
EDP = 16A

3.3V G3H Regulator
EDP = 22A

PAGE TITLE		
PLATFORM POWER: 3.3V G3H/5V G3S VR		
 Apple Inc.	DRAWING NUMBER	051-04705
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BOM_COST_GROUP=PLATFORM POWER

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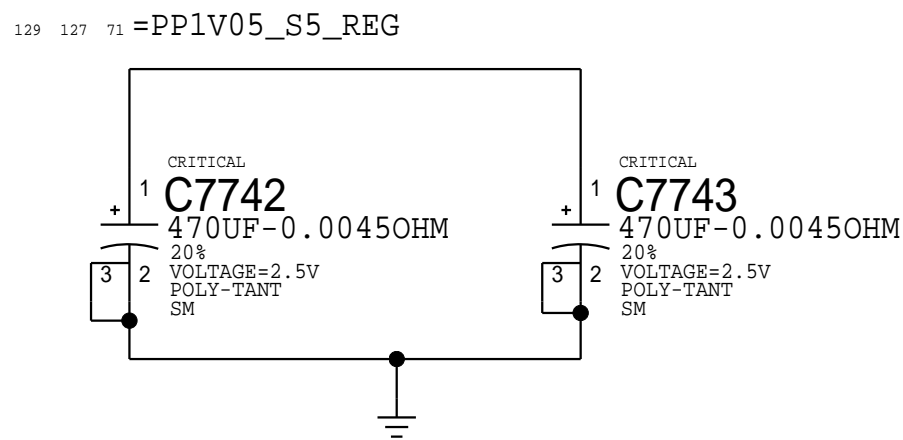
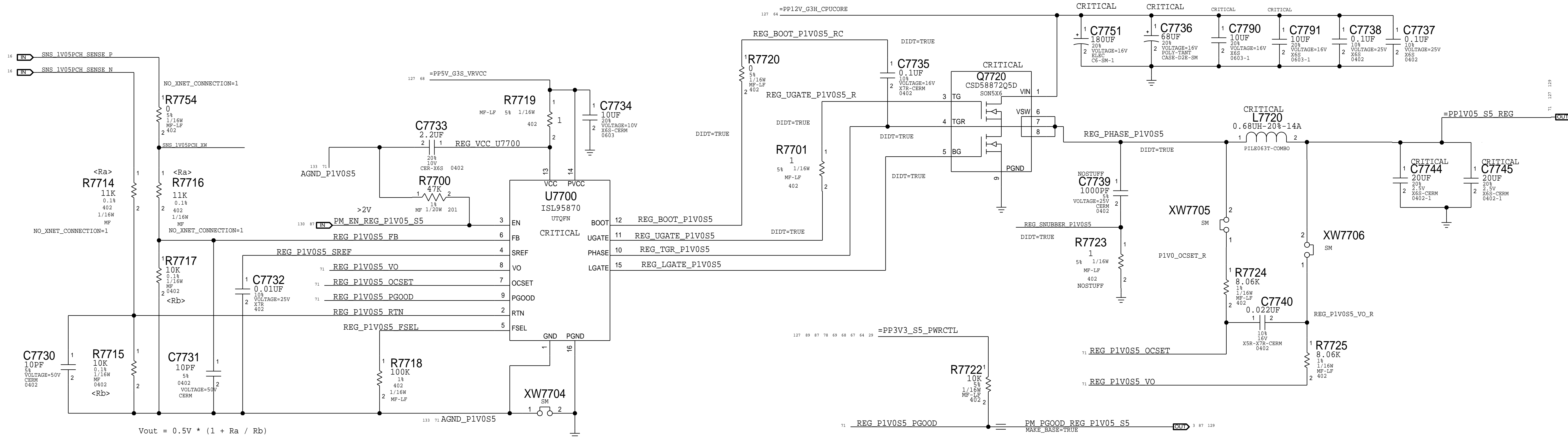
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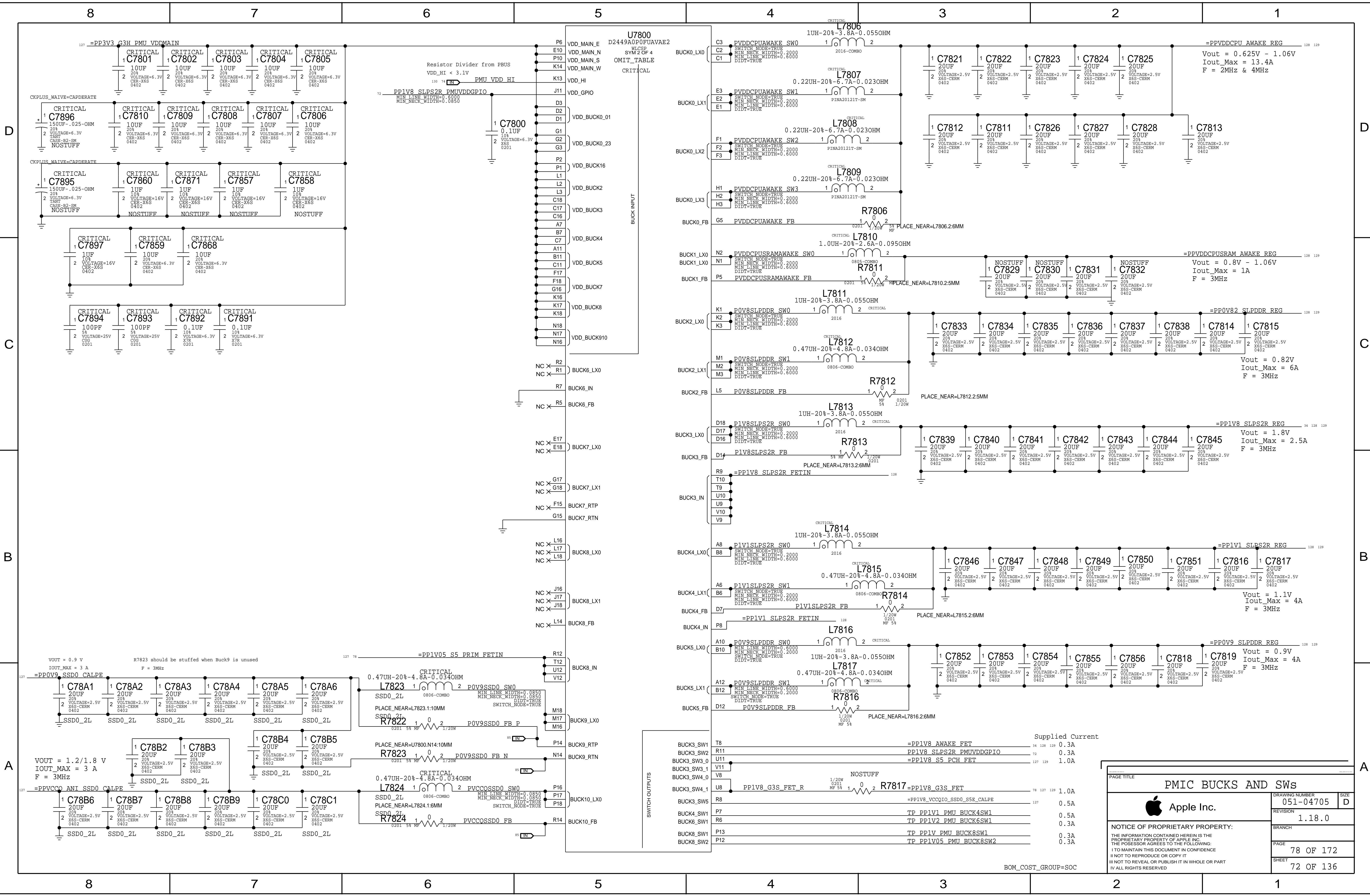
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PCH 1V05 SUPPLY
EDP = 6A
VOUT = 1.05V




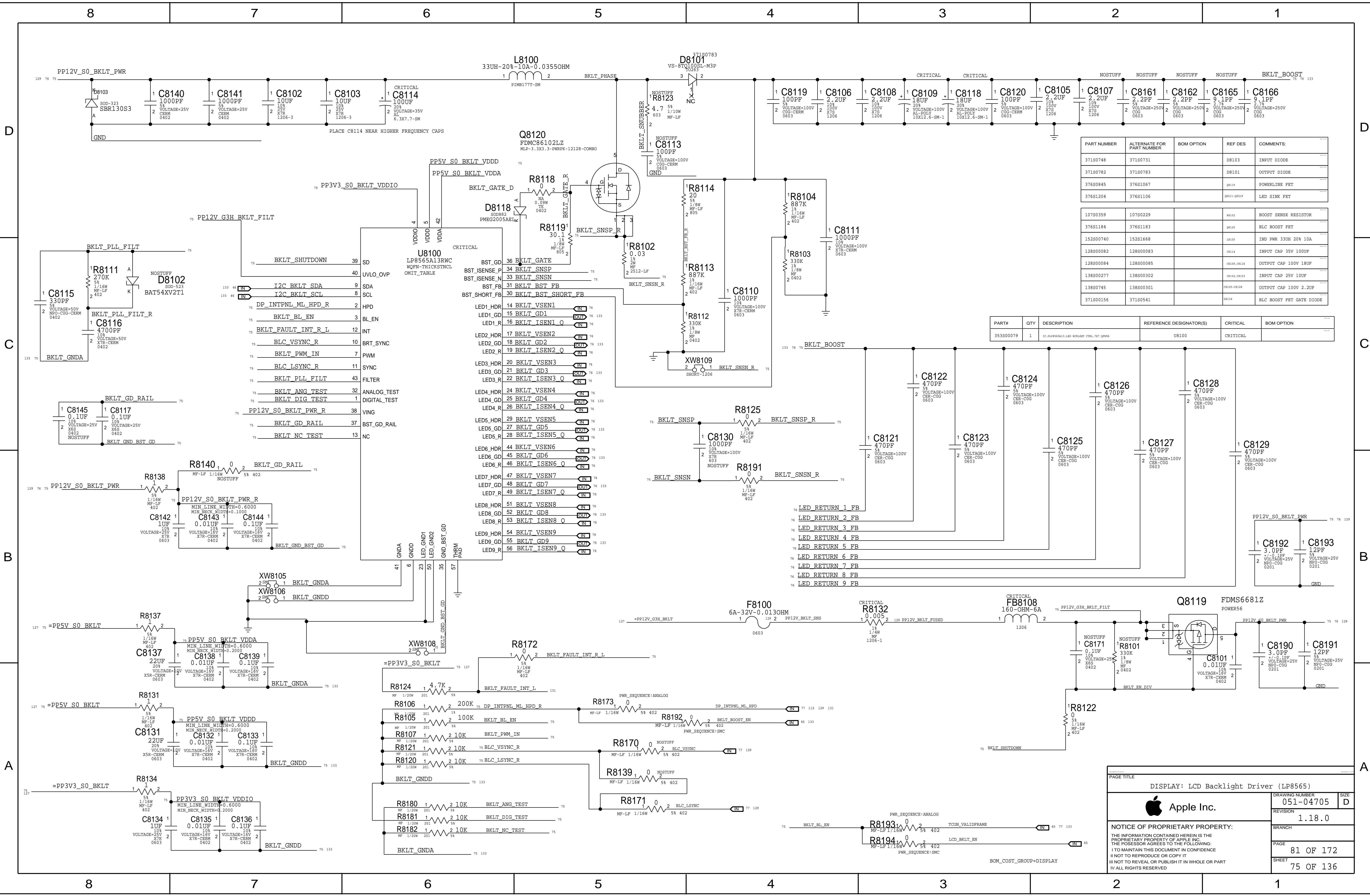
PAGE TITLE		
CPU & CHIPSET: PCH 1V05		
 Apple Inc.	DRAWING NUMBER	051-04705
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BOM_COST_GROUP=CPU & CHIPSET



BOM_COST_GROUP=SOC

PAGE TITLE		
PMIC BUCKS AND SWs		
 Apple Inc.	DRAWING NUMBER	051-04705
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0748	371S0731		D8103	INPUT DIODE
371S0782	371S0783		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8211-Q8219	LED SINK FET
107S0359	107S0229		R8102	BOOST SENSE RESISTOR
376S1184	376S1183		Q8120	BLC BOOST FET
152S00740	152S1668		C8100	IND FWR 33UH 20% 10A
128S00082	128S00083		C8114	INPUT CAP 35V 100UF
128S00084	128S00085		C8109,C8118	OUTPUT CAP 100V 18UF
138S00277	138S00302		C8102,C8103	INPUT CAP 25V 10UF
138S0745	138S00301		C8105-C8108	OUTPUT CAP 100V 2.2UF
371S00156	371S0541		D8118	BLC BOOST FET GATE DIODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S00079	1	IC,LP8565A13,LED BACKLIGHT CTRL,727 QFN56	U8100	CRITICAL	

PAGE TITLE			
DISPLAY: LCD Backlight Driver (LP8565)			
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051-04705		D	
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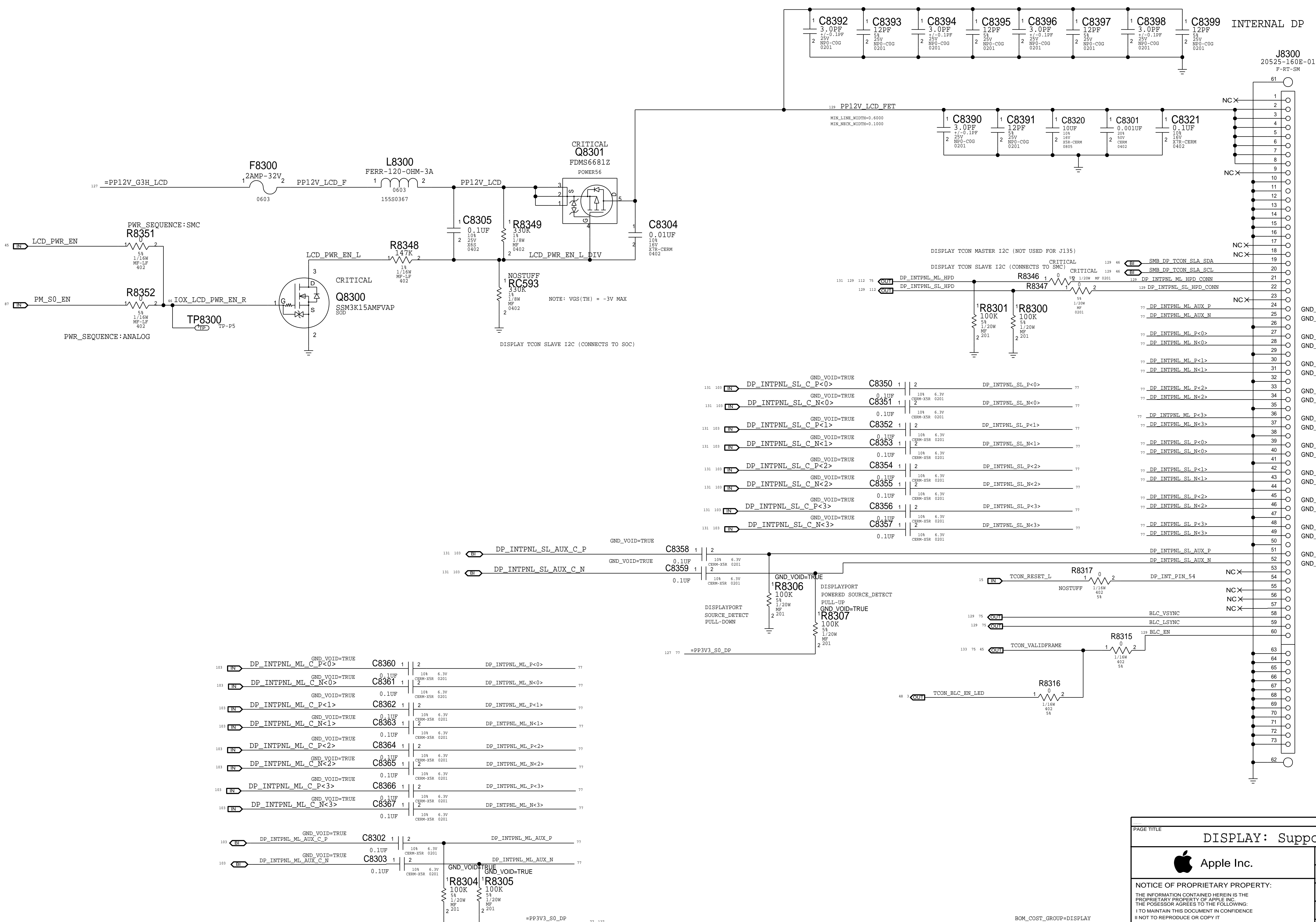
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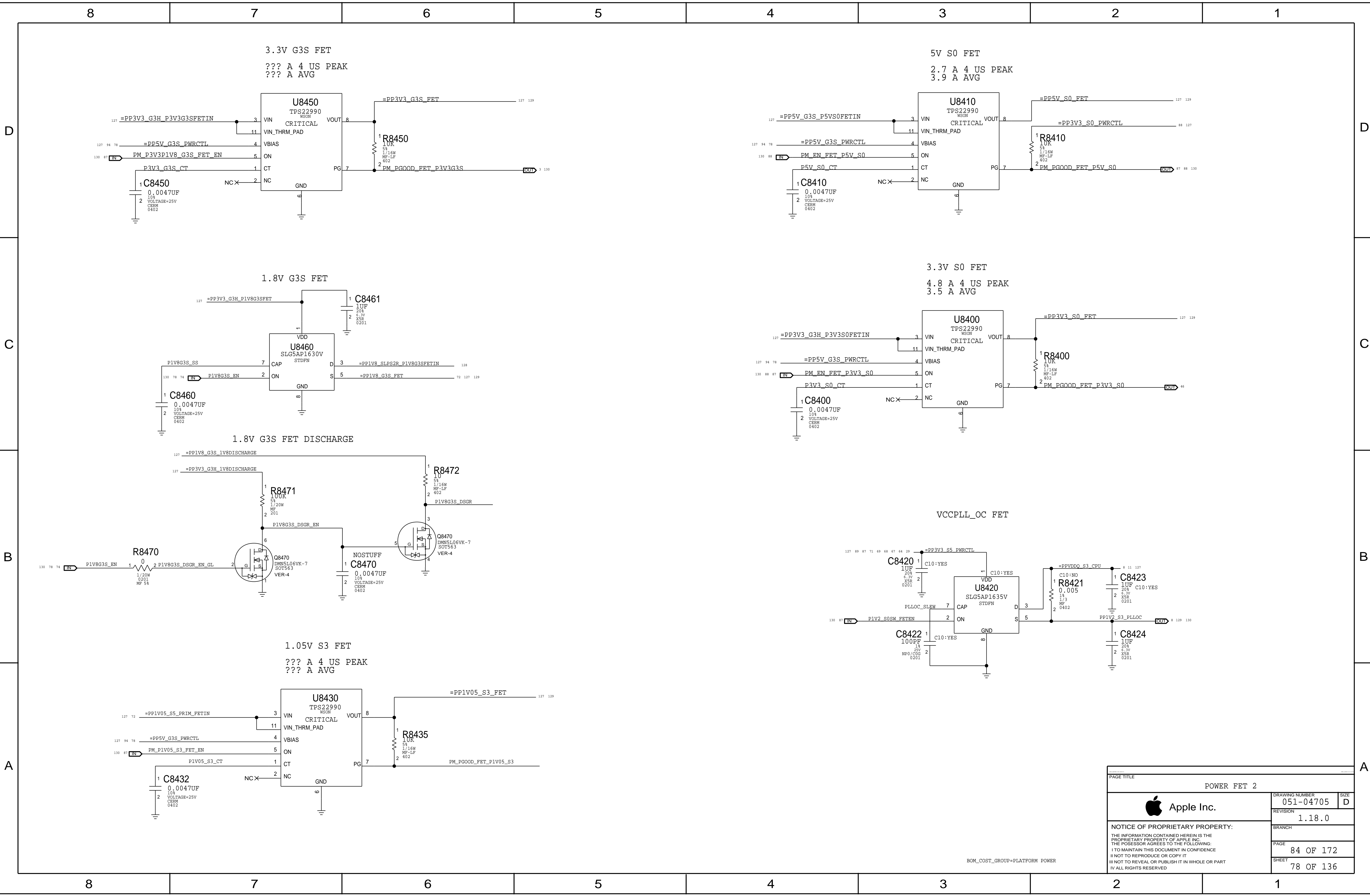
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PAGE TITLE			
DISPLAY: Support			
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BOM_COST_GROUP=DISPLAY



PAGE TITLE			
POWER FET 2			
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BOM_COST_GROUP=PLATFORM POWER

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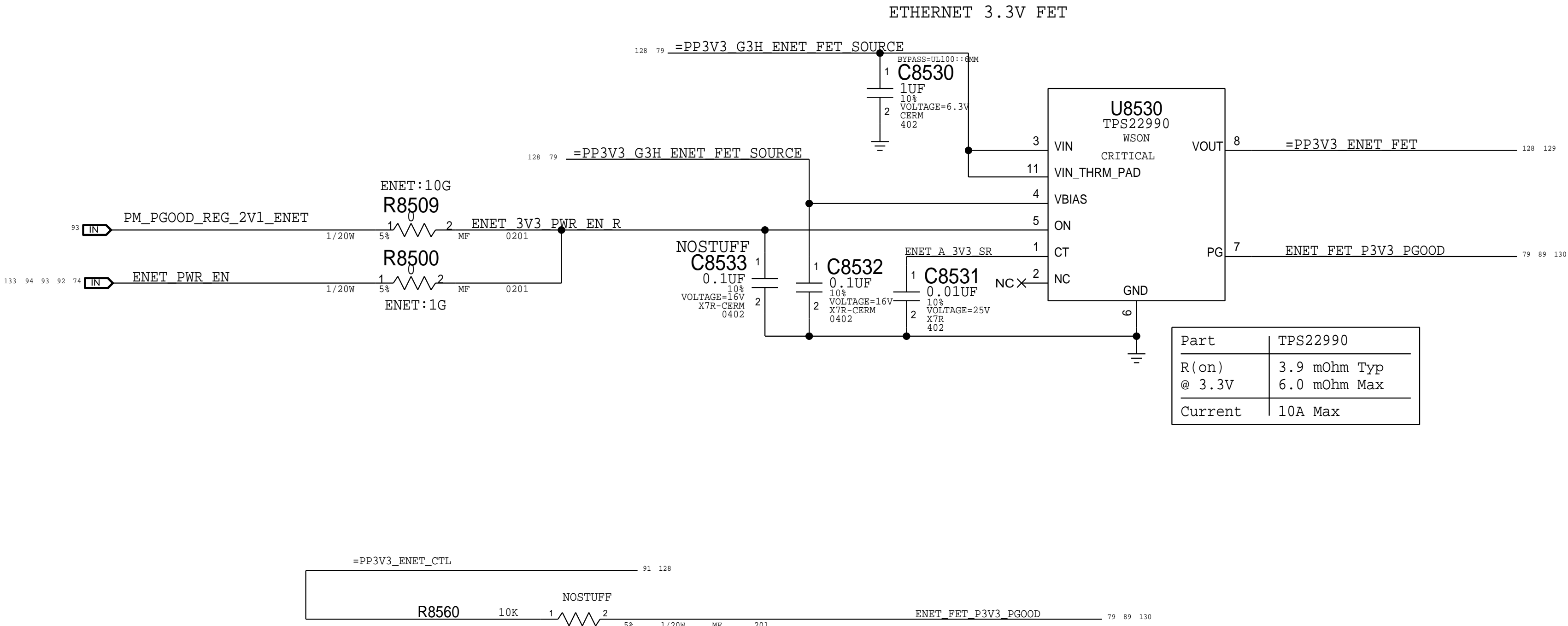
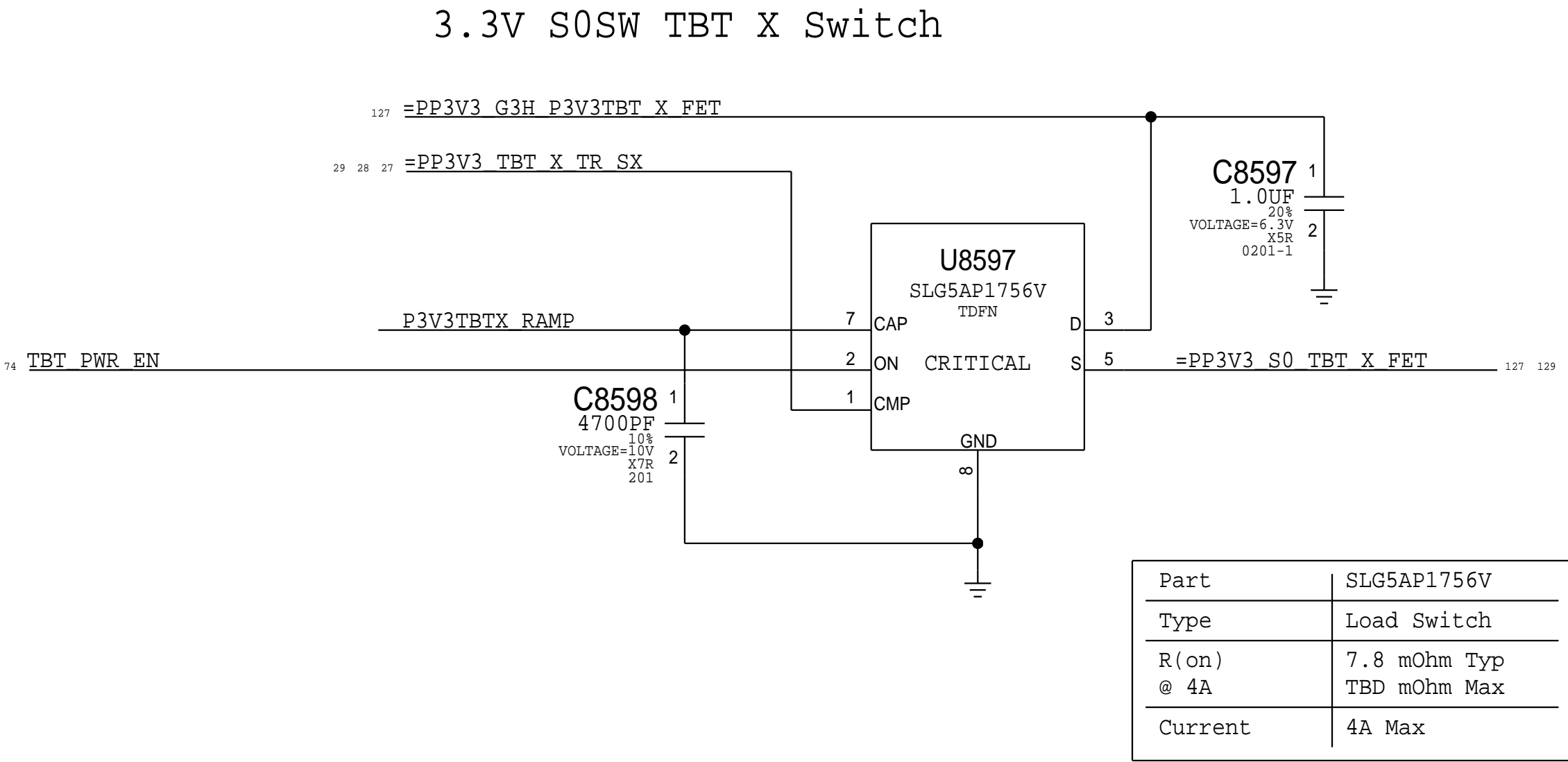
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System Power States

System State:	Shutdown (G3H)		Standby (G3S)		Standby (S4)		Sleep (S3/S0i)		Run (S0)
CPU/PCH State:	Off (RTC Only)		Off (RTC Only)		Standby		Sleep		Run
Rails	SoC State:		S2R	Awake	S2R	Awake	S2R	Awake	Awake
PP*_S2R (0.8,1.1,1.8V)			On	On	On	On	On	On	On
PP*_DDR (0.8,0.9,1.1V)			Off	On	Off	On	Off	On	On
PP*_AWAKE (CPU,SRAM,1.2,1.8,3.3V)			Off	On	Off	On	Off	On	On
PP3V3_G3H (VR1)			On	On	On	On	On	On	On
PP3V3_G3H (VMAIN)			On	On	On	On	On	On	On
PP*_G3S (1.8,3.3,5V)			Off	On	On	On	On	On	On
PP*_S5 (1.8,3.3V)			Off	Off	Off	On	On	On	On
CPU VRs			Off	Off	Off	Off	Off/On	Off/On	On
PCH VRs			Off	Off	Off	On	On	On	On
DDR4 VRs			Off	Off	Off	Off	SR	SR	On
GPU VRs/BLC/DISPLAY			Off	Off	Off	Off	Off	Off	On

* System: Shutdown Awake is a transition state only.
* SoC: SLP_DDR is a transition state only.
* CPU/PCH: S4 is only used by desktops for USB wakes.
* CPU/PCH: S5 is a transition state. May also be used for RTC wakes.
* SR:Self Refresh



POWER FET

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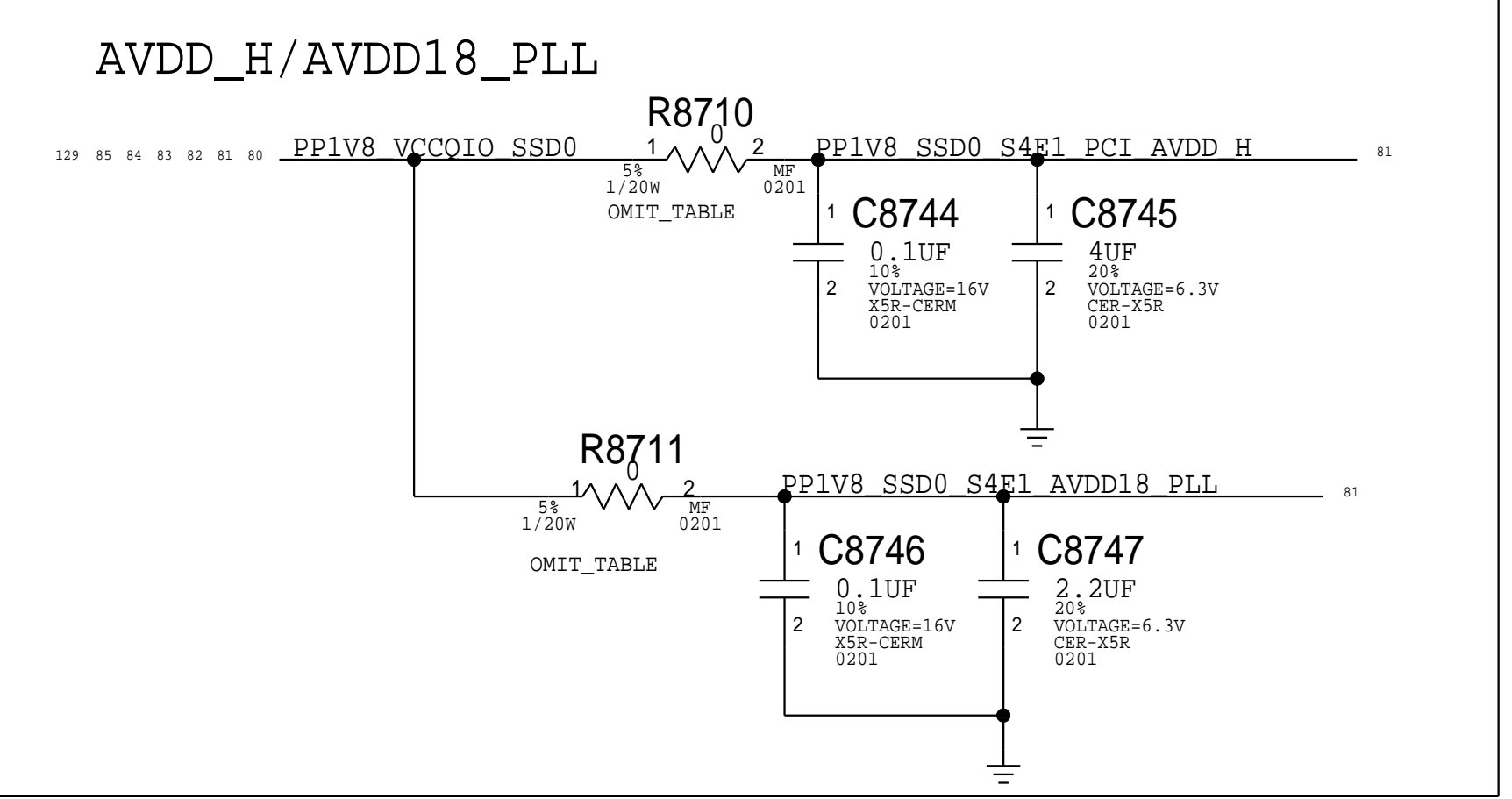
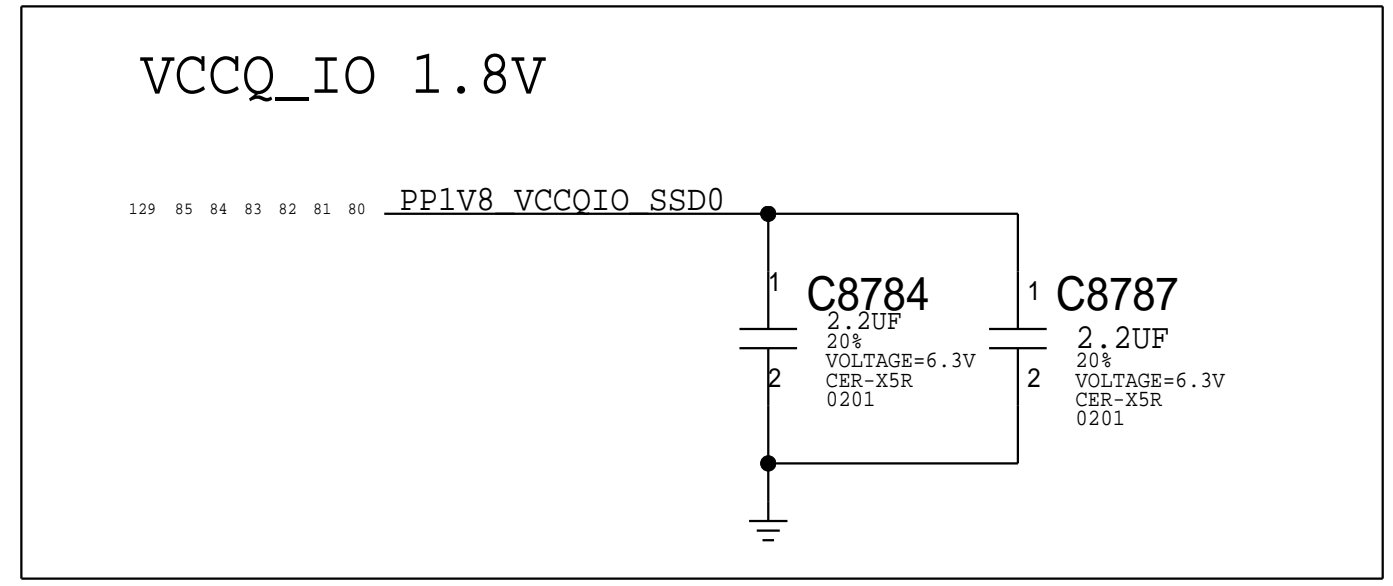
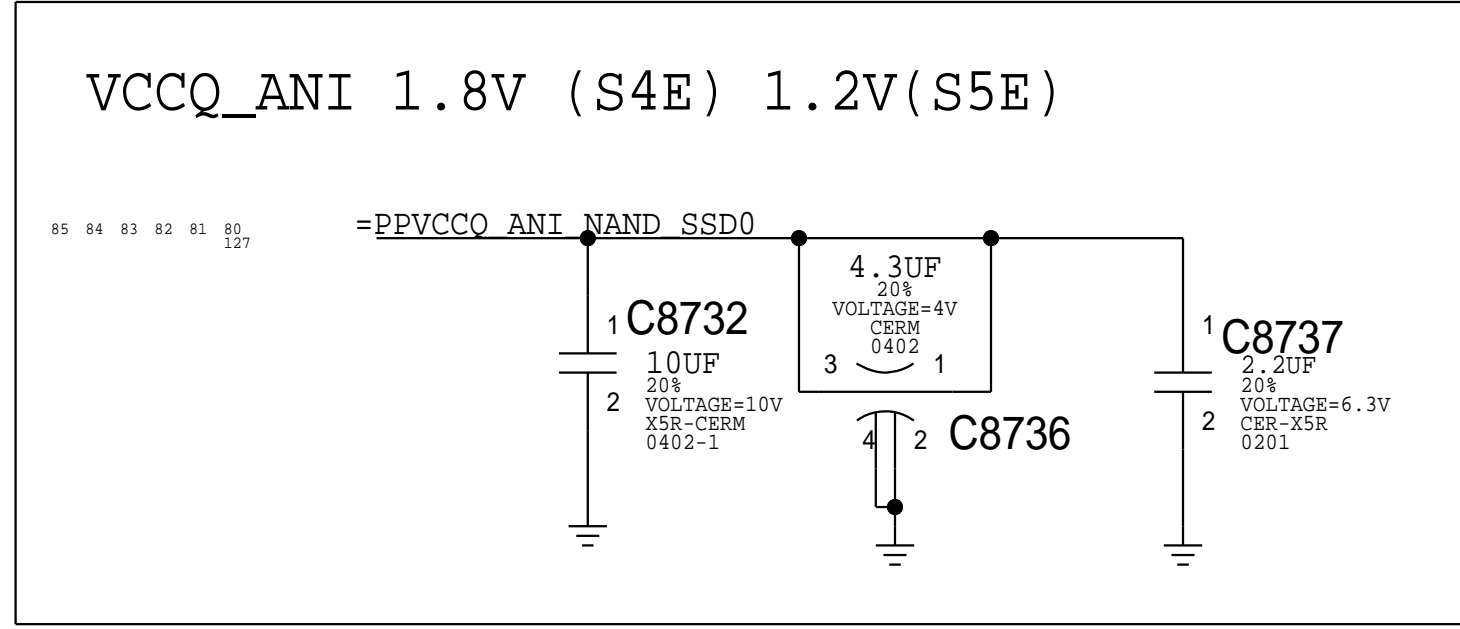
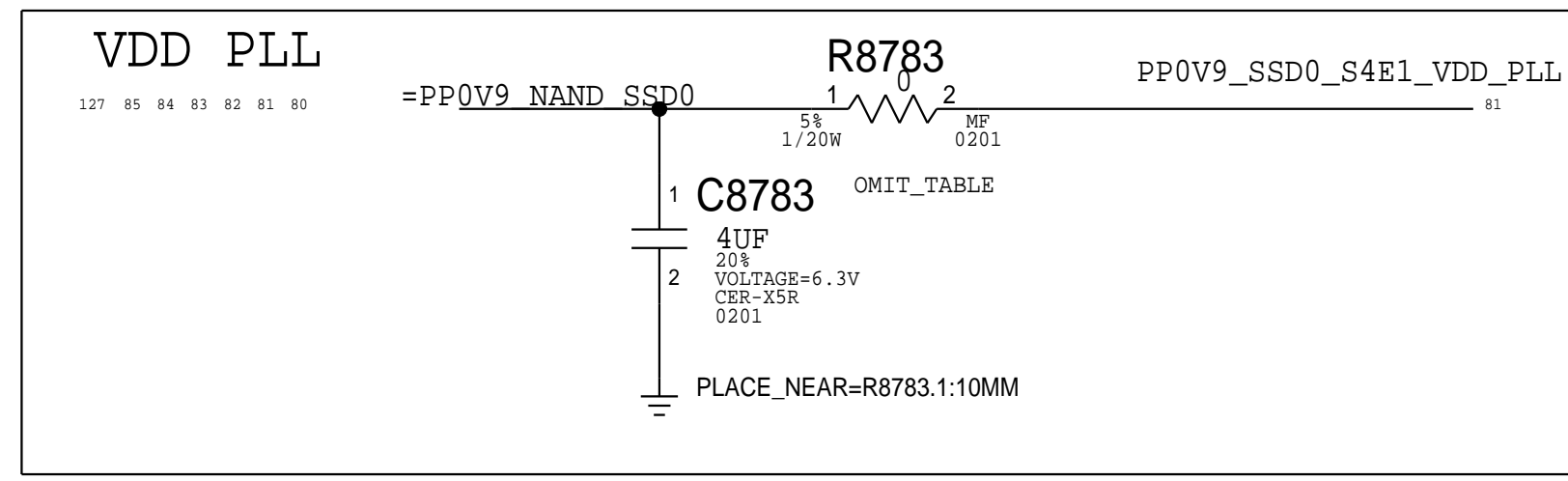
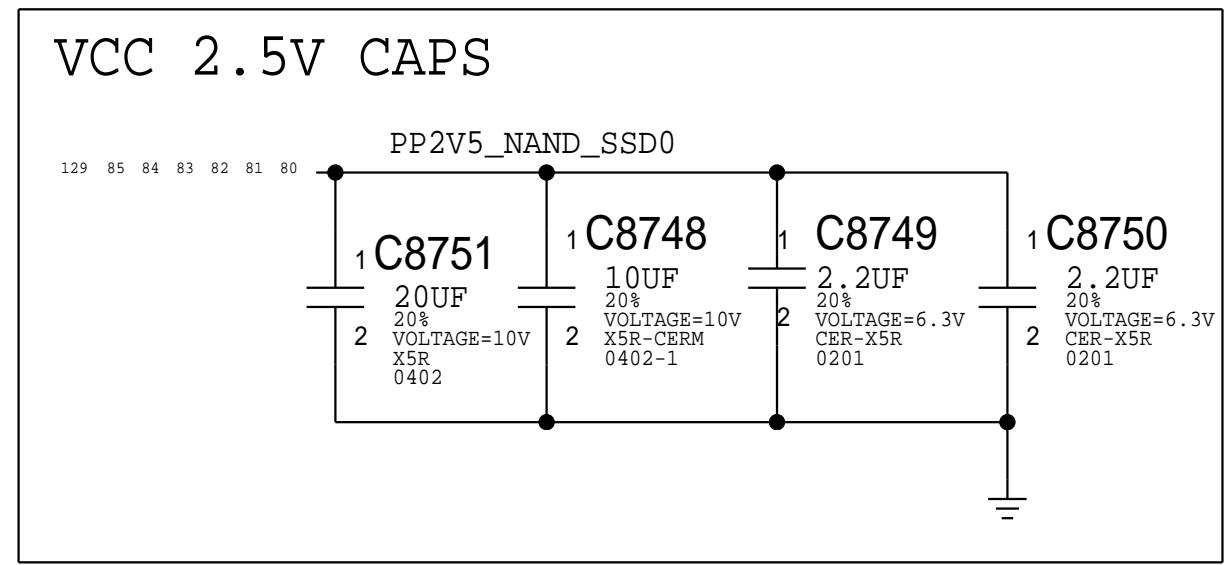
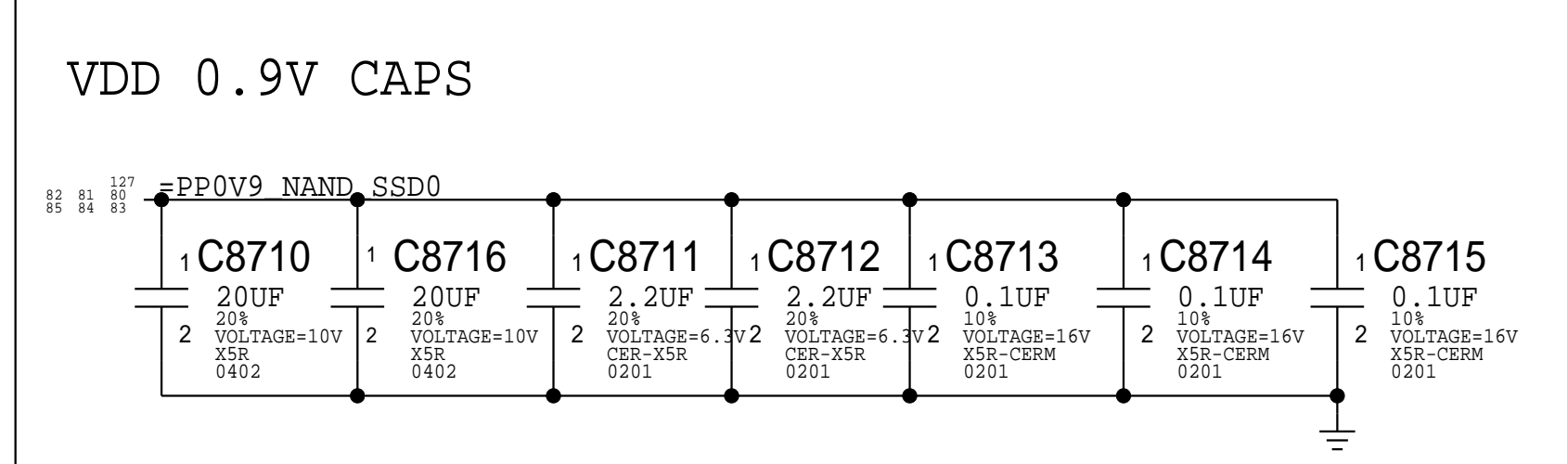
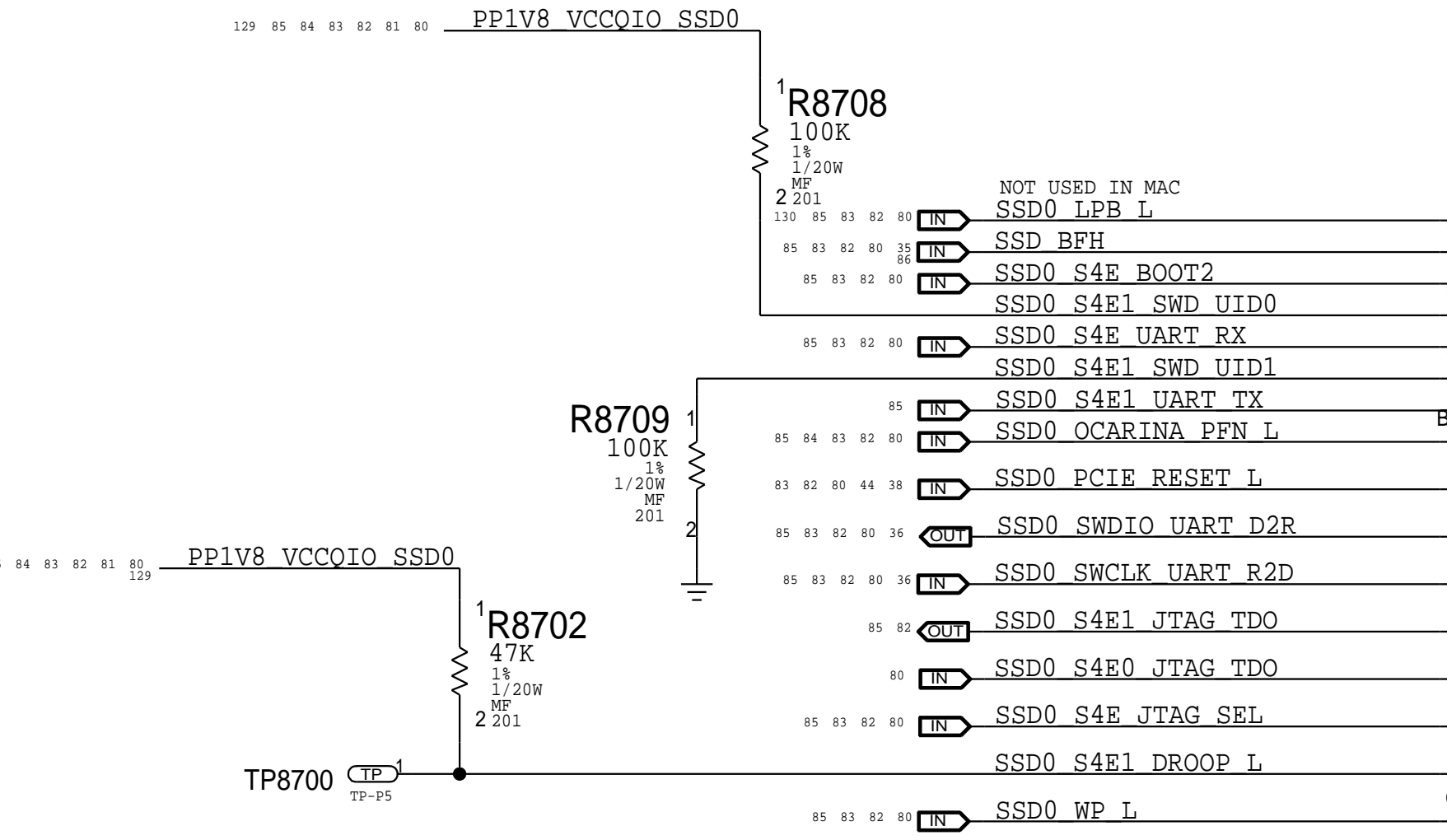
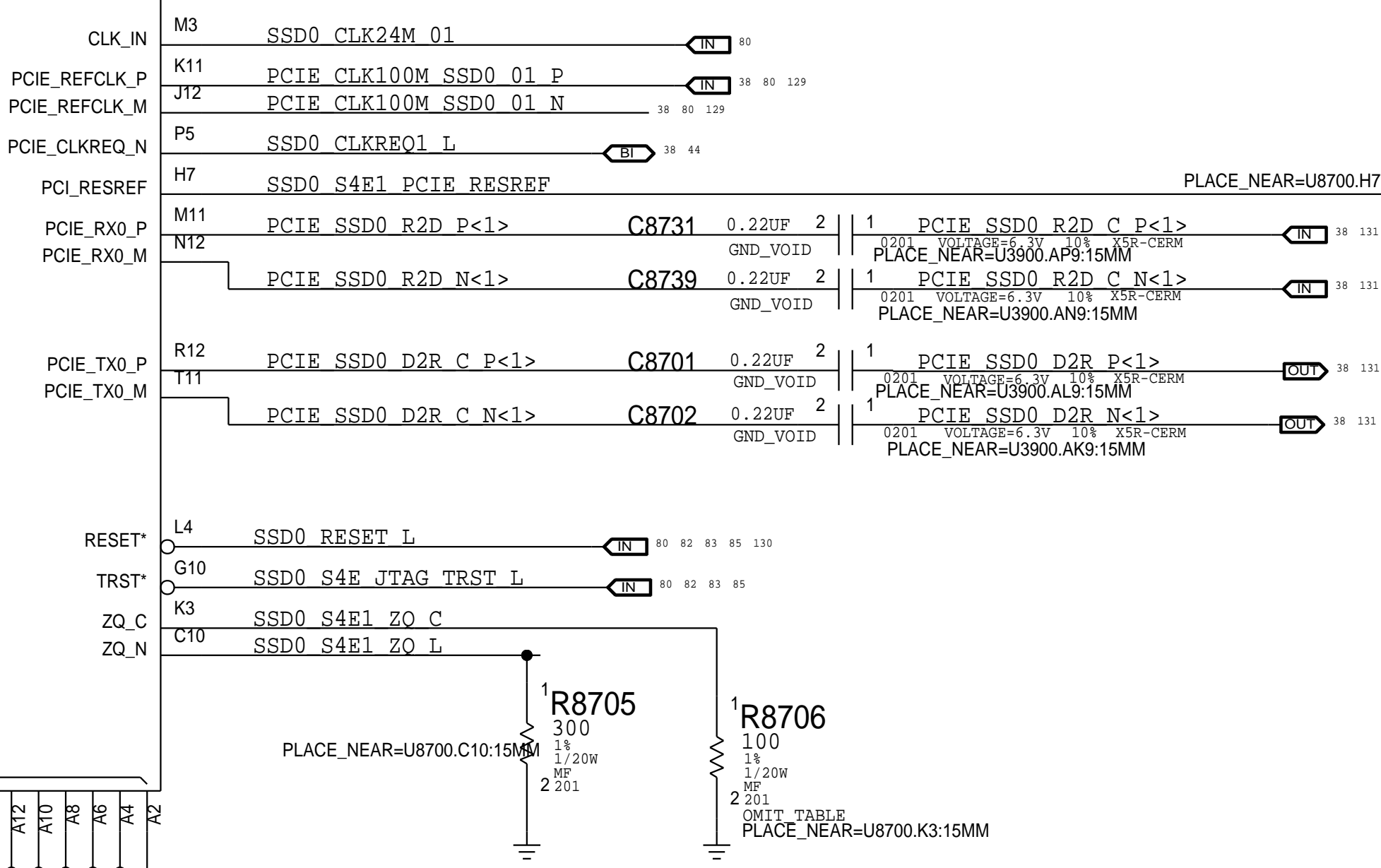
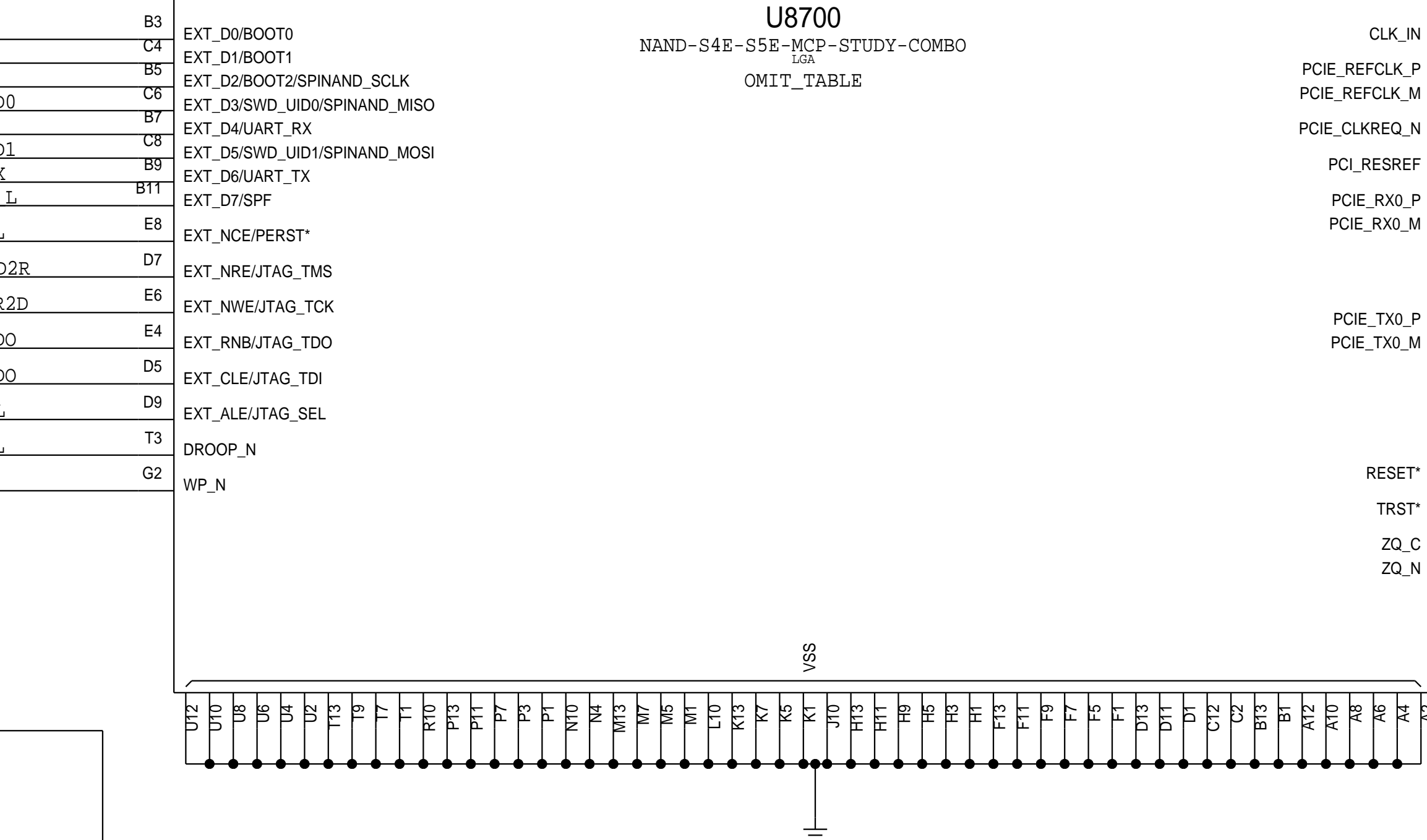
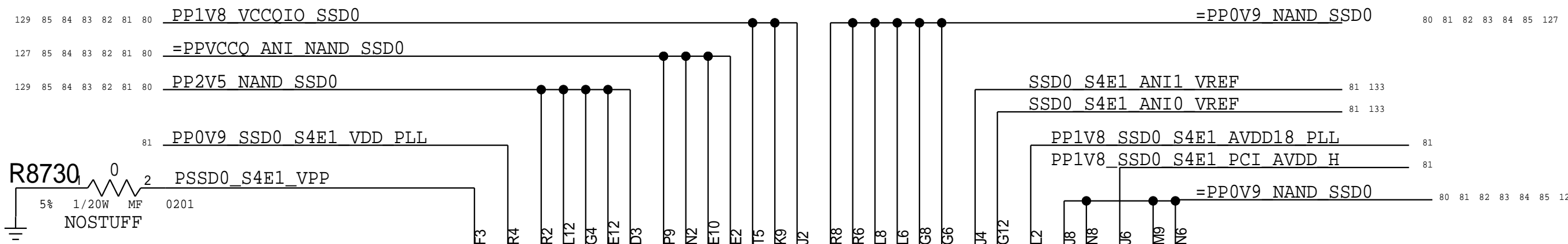
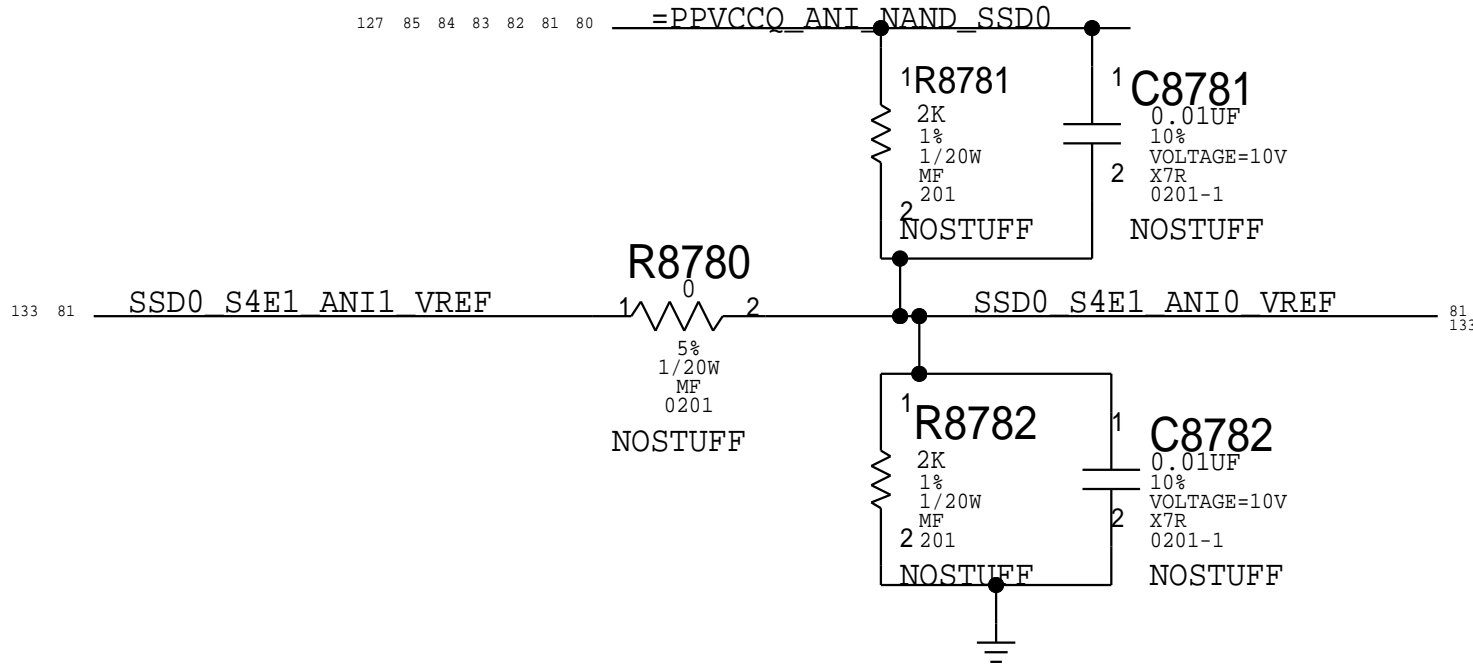
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D

SSD0 S4E1/S5E1

EXTERNAL VREF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0279	1	RES, 3.01KOHM,1%,1/20W,0201	R8704	CRITICAL	SSD0_S4E
103S00429	1	RES, 200OHM,0.1%,1/20W,0201	R8704	CRITICAL	SSD0_S5E
118S0011	1	RES, 100OHM,1%,1/20W,0201	R8705	CRITICAL	SSD0_S4E
118S0273	1	RES, 300OHM,1%,1/20W,0201	R8706	CRITICAL	SSD0_S5E
117S0201	2	RES, 0OHM,1/20W,0201	R8783,R8710,R8711	CRITICAL	SSD0_S4E
155S00161	2	FERR BD, 100HM,0.05 DCR,0201	R8783,R8710	CRITICAL	SSD0_S5E
118S0794	1	RES, MF, 20HM,1%,1/20W,0201	R8711	CRITICAL	SSD0_S5E

SSD0: S4E/S5E<1>

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BOM_COST_GROUP=SSD

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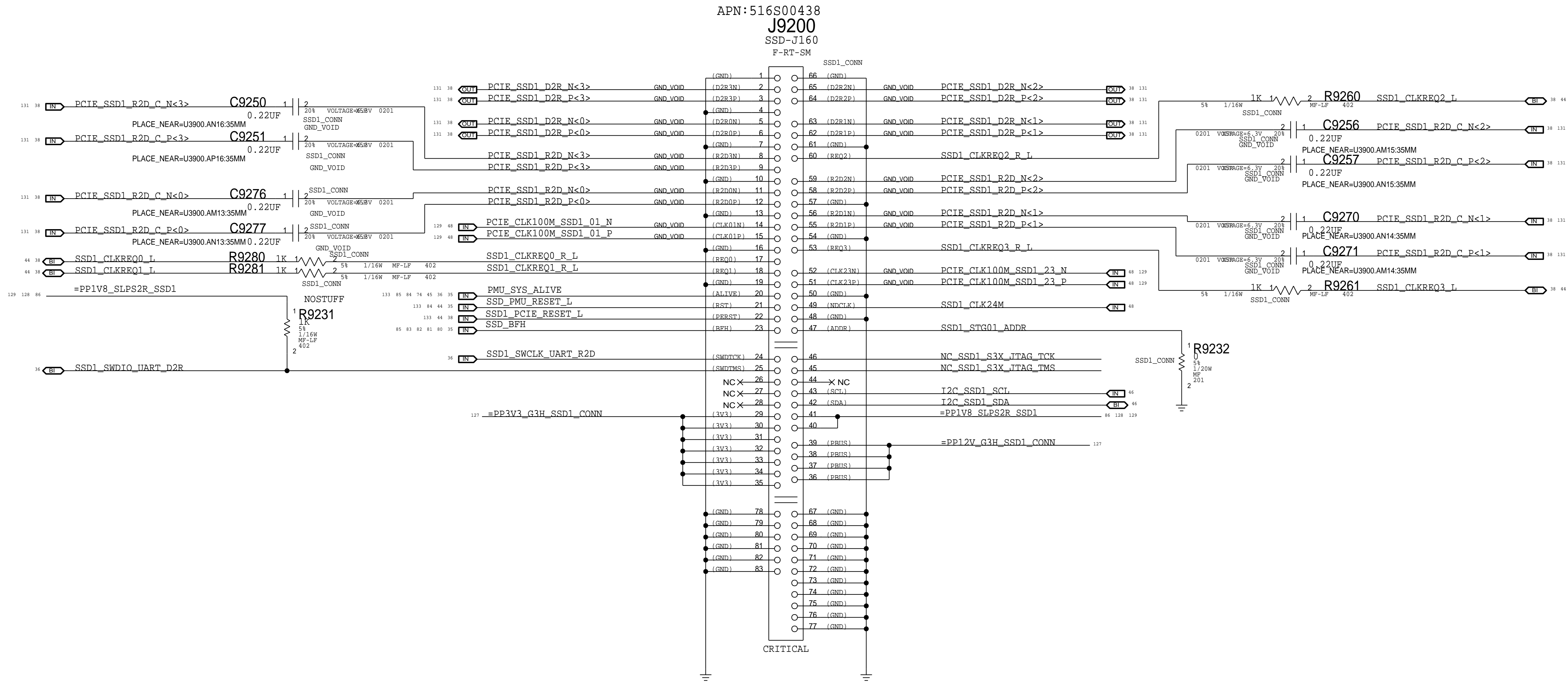
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SSD1 GS5 CONNECTOR



BOM_COST_GROUP=SSD

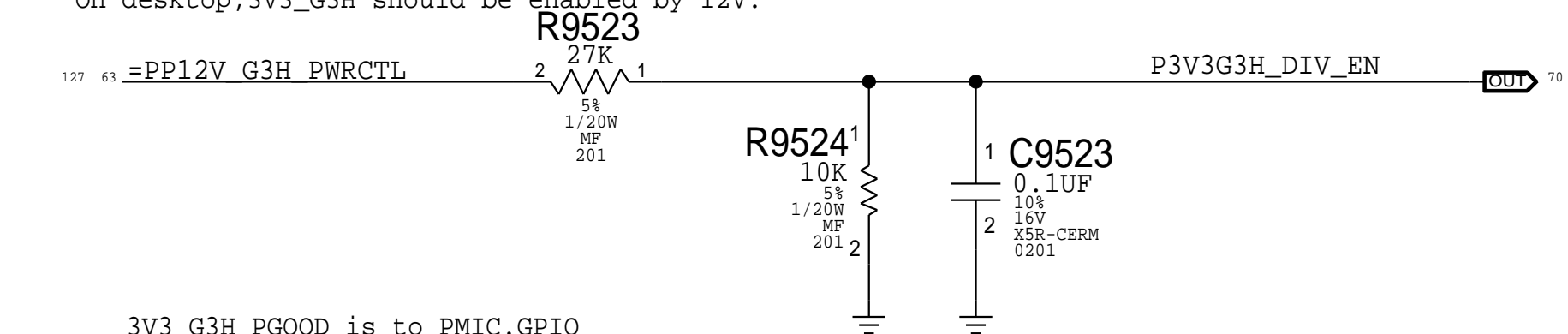
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SSD 1 CONN		
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G3H

12V_G3H uses ACDC

3V3_G3H is enabled by PMIC.PVDDMAIN_EN - this is only applied for laptop Big current G3H.

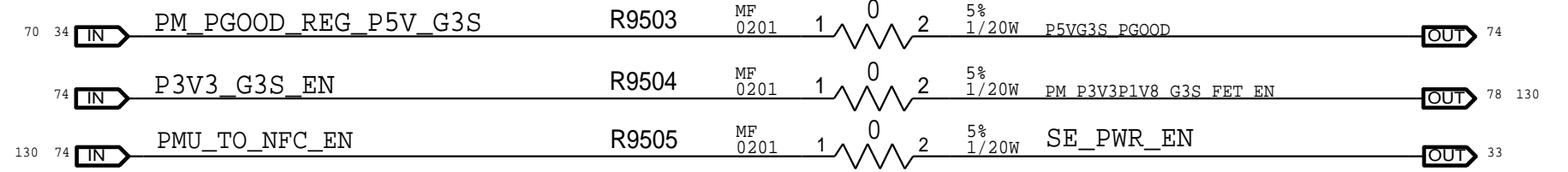
On desktop,3V3_G3H should be enabled by 12V.



3V3_G3H_PGOOD is to PMIC.GPIO

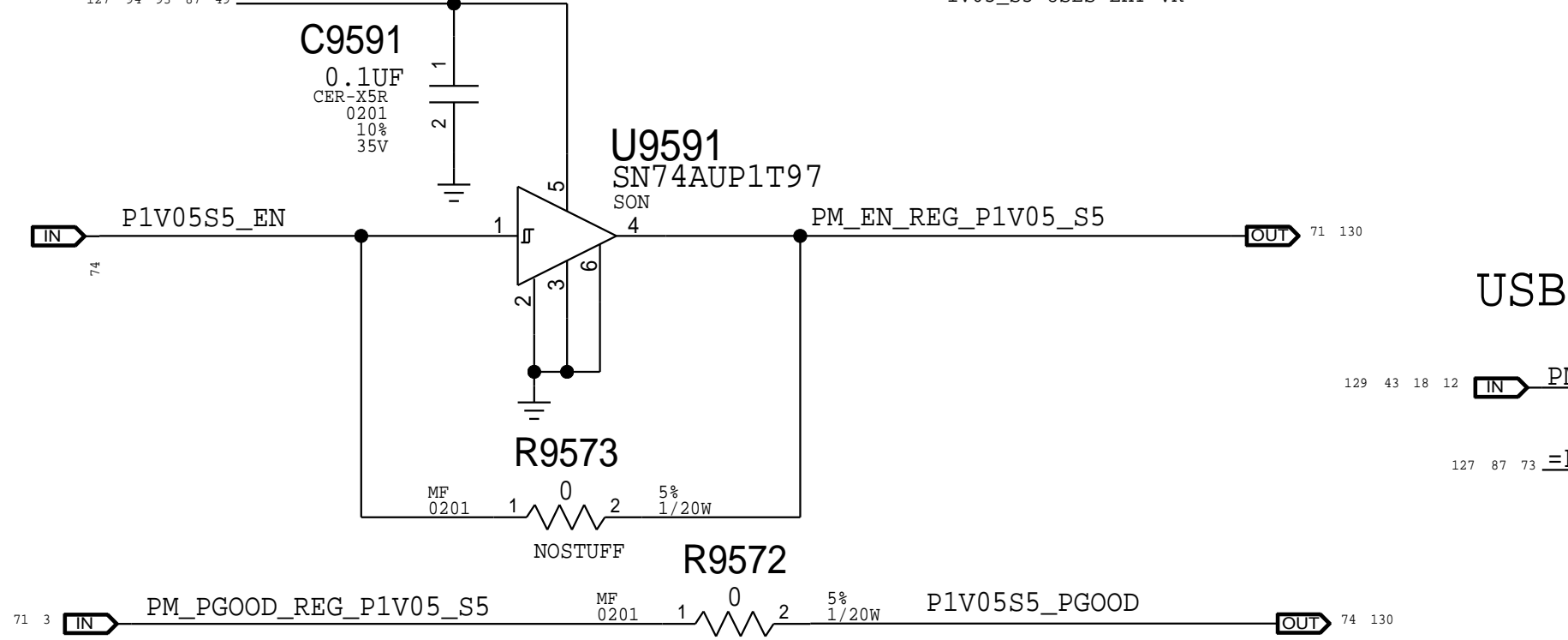
G3S

- static timing by PMU



S5

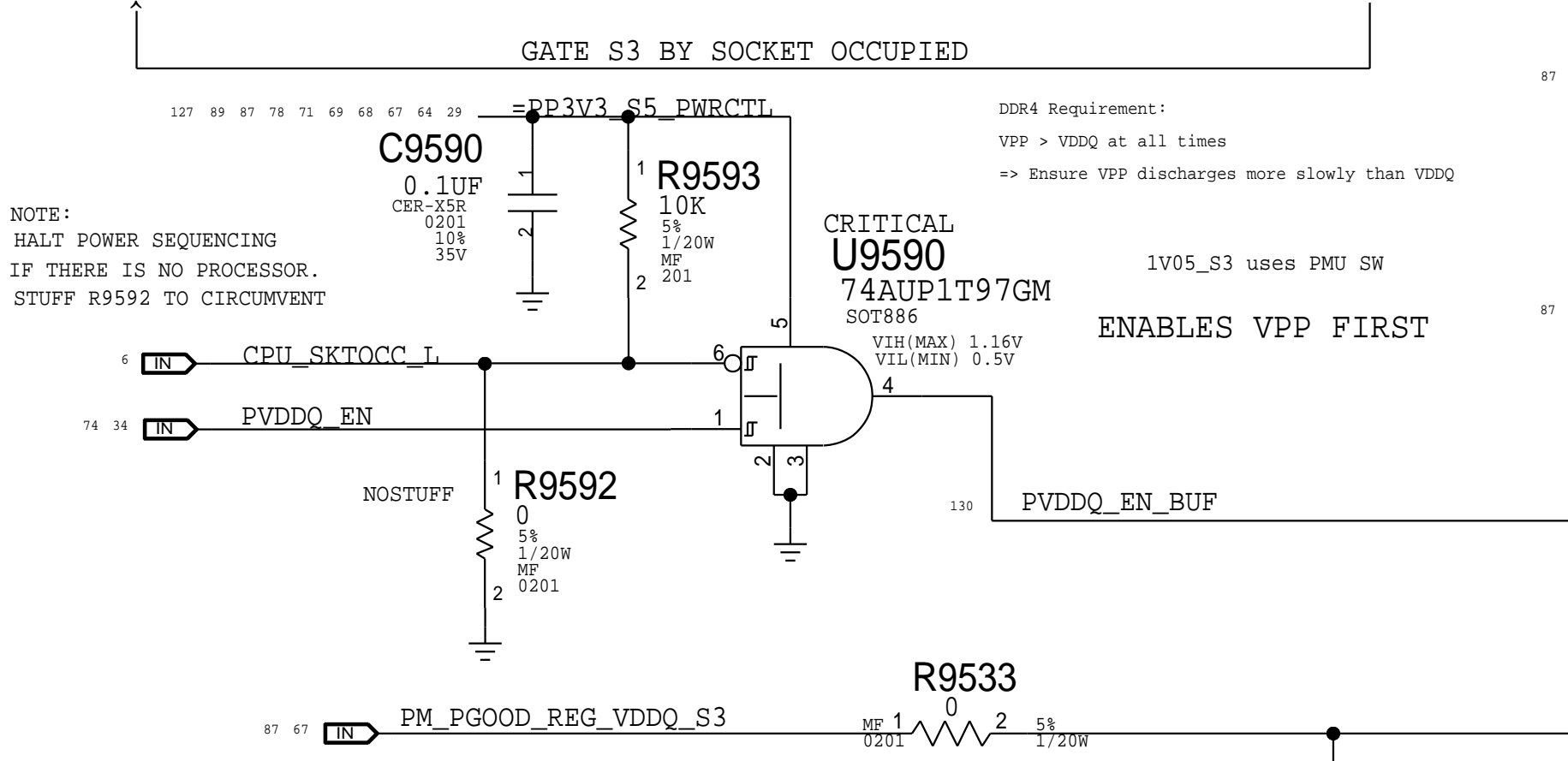
- static timing by PMU



S3

1V2_S3 sequencing

Calpe VDDQ_EN -> 2V5_VTT -> 2V5_PGOOD -> Enable 1V2 VDDQ -> VDDQ_PGDD



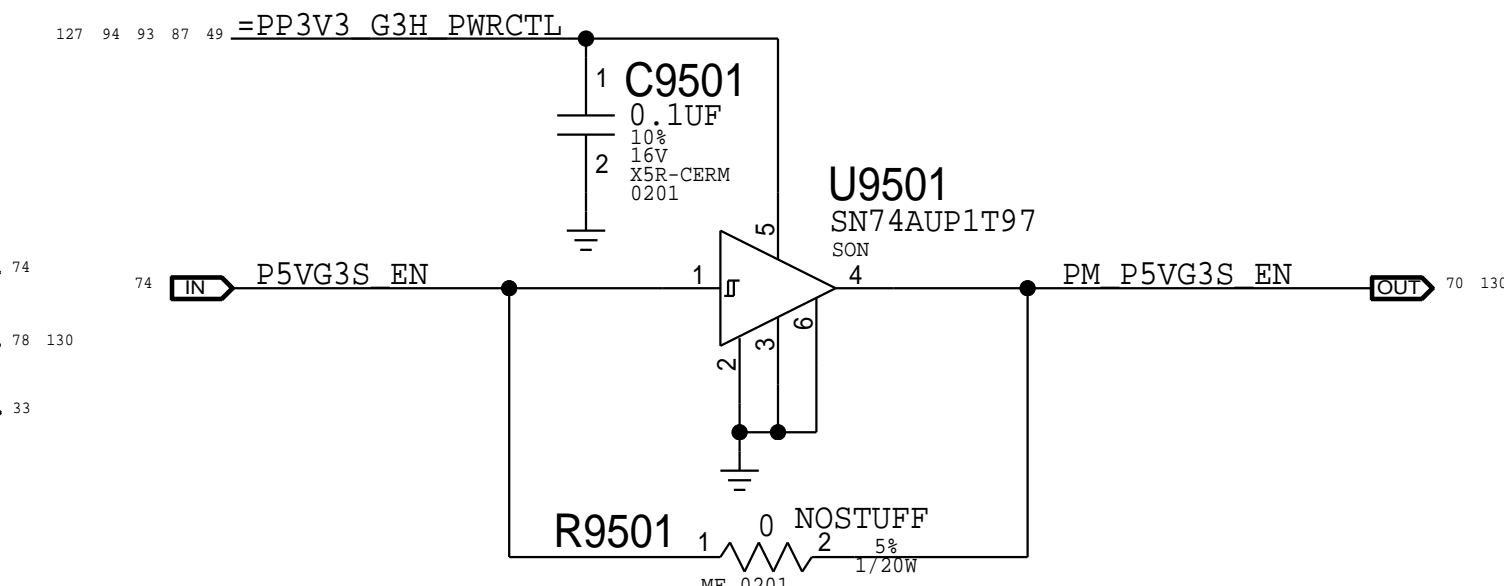
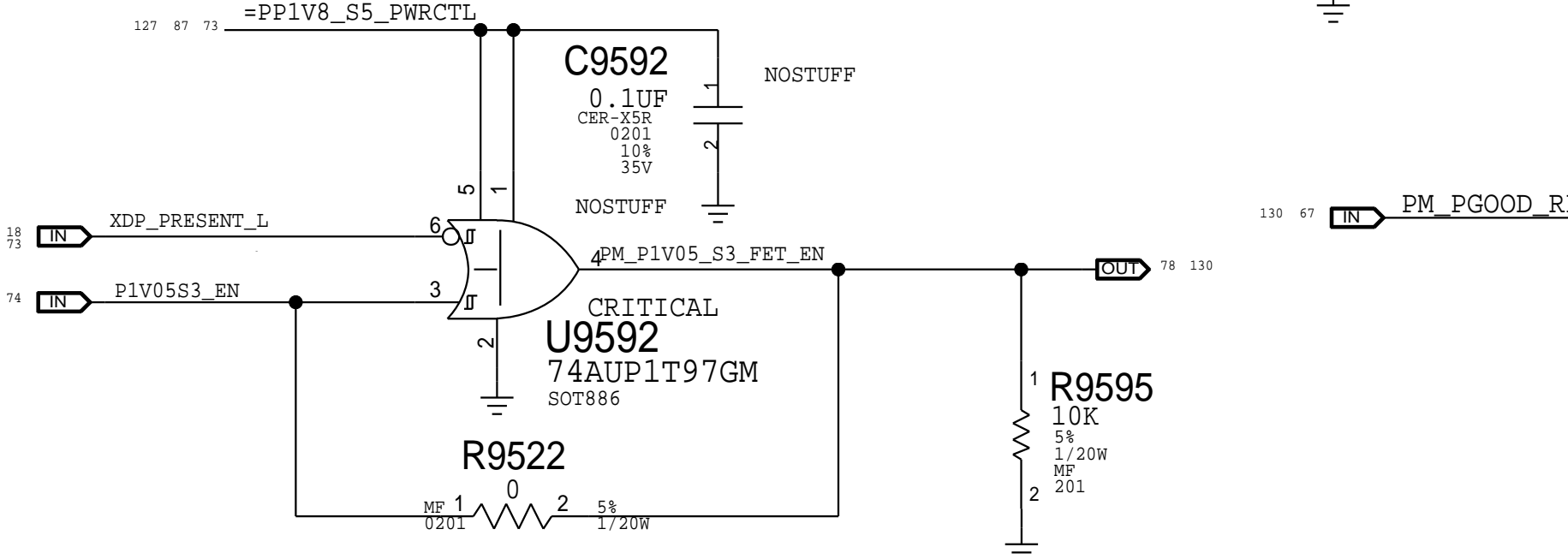
NOTE:
HALT POWER SEQUENCING
IF THERE IS NO PROCESSOR.
STUFF R9592 TO CIRCUMVENT

DDR4 Requirement:
VPP > VDDQ at all times
=> Ensure VPP discharges more slowly than VDDQ

1V05_S3 uses PMU SW

ENABLES VPP FIRST

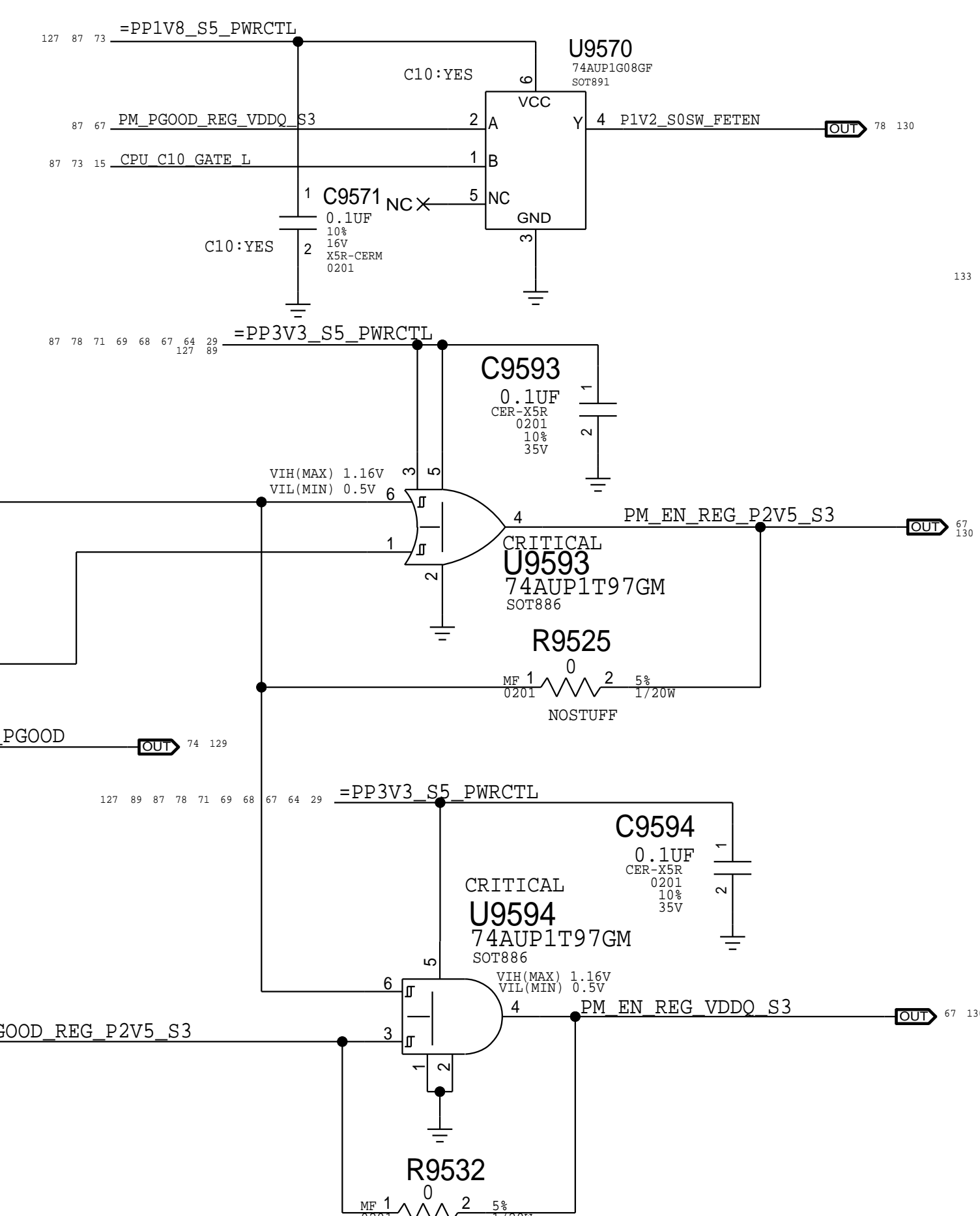
XDP PRESENT POWER OVERRIDE



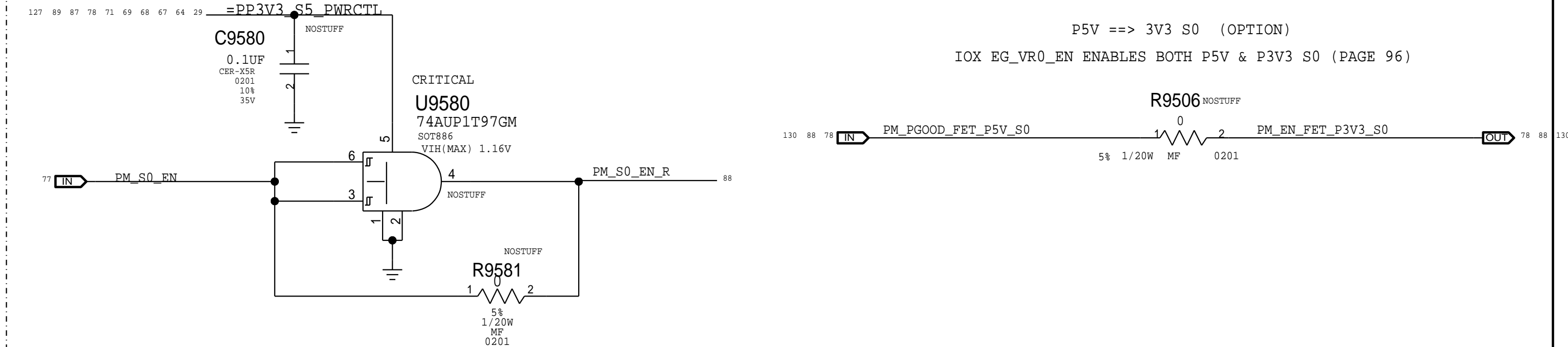
USB-A

- HW sequencing

VCCPLL_OC SEQUENCING



3V3 AND 5V S0 FOR GPU + DISPLAY + BLC

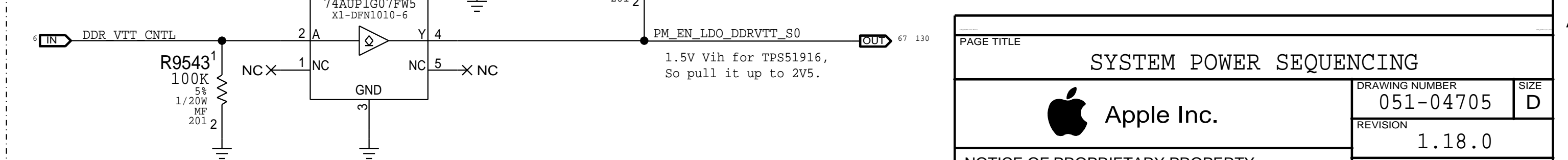
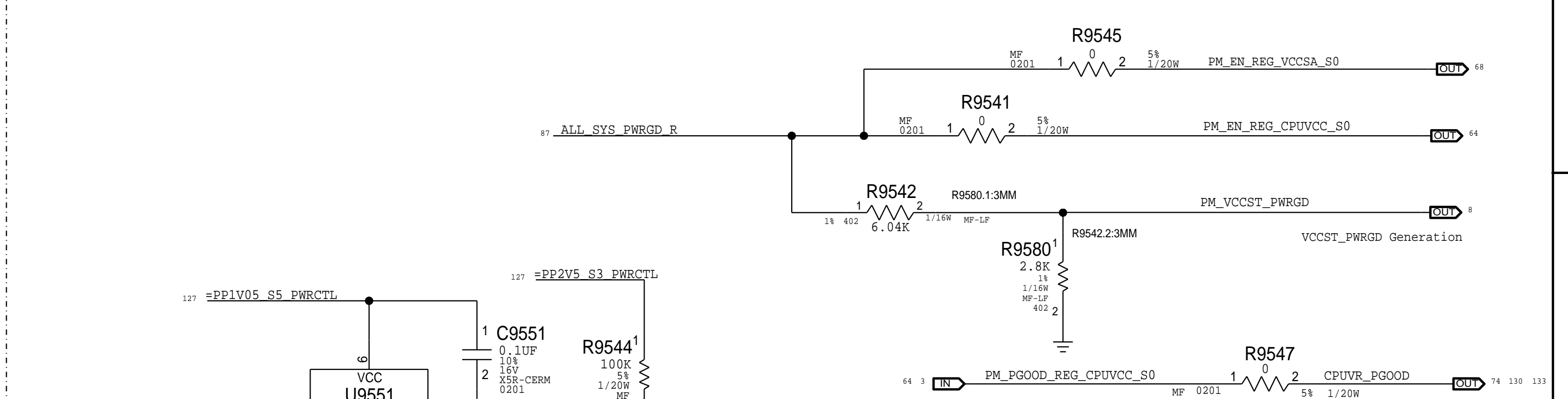
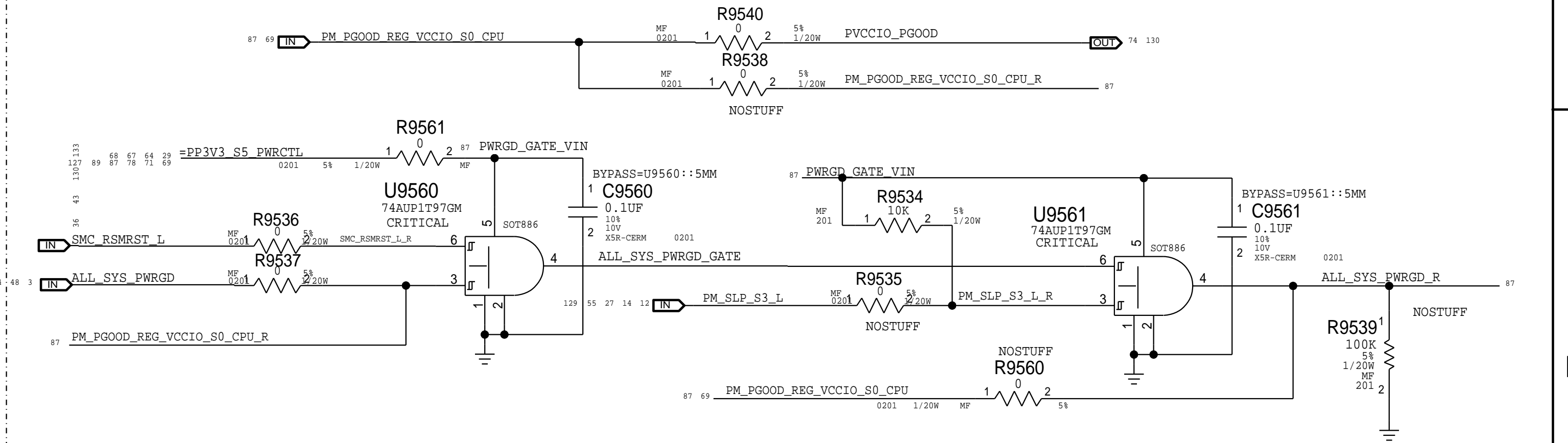
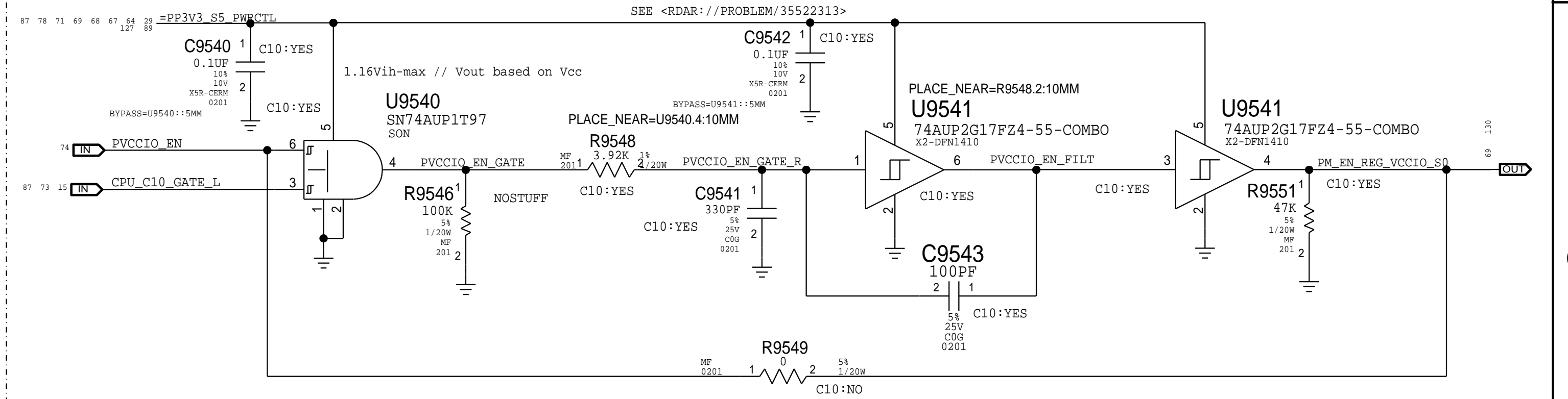


P5V ==> 3V3 S0 (OPTION)

IOX EG_VR0_EN ENABLES BOTH P5V & P3V3 S0 (PAGE 96)

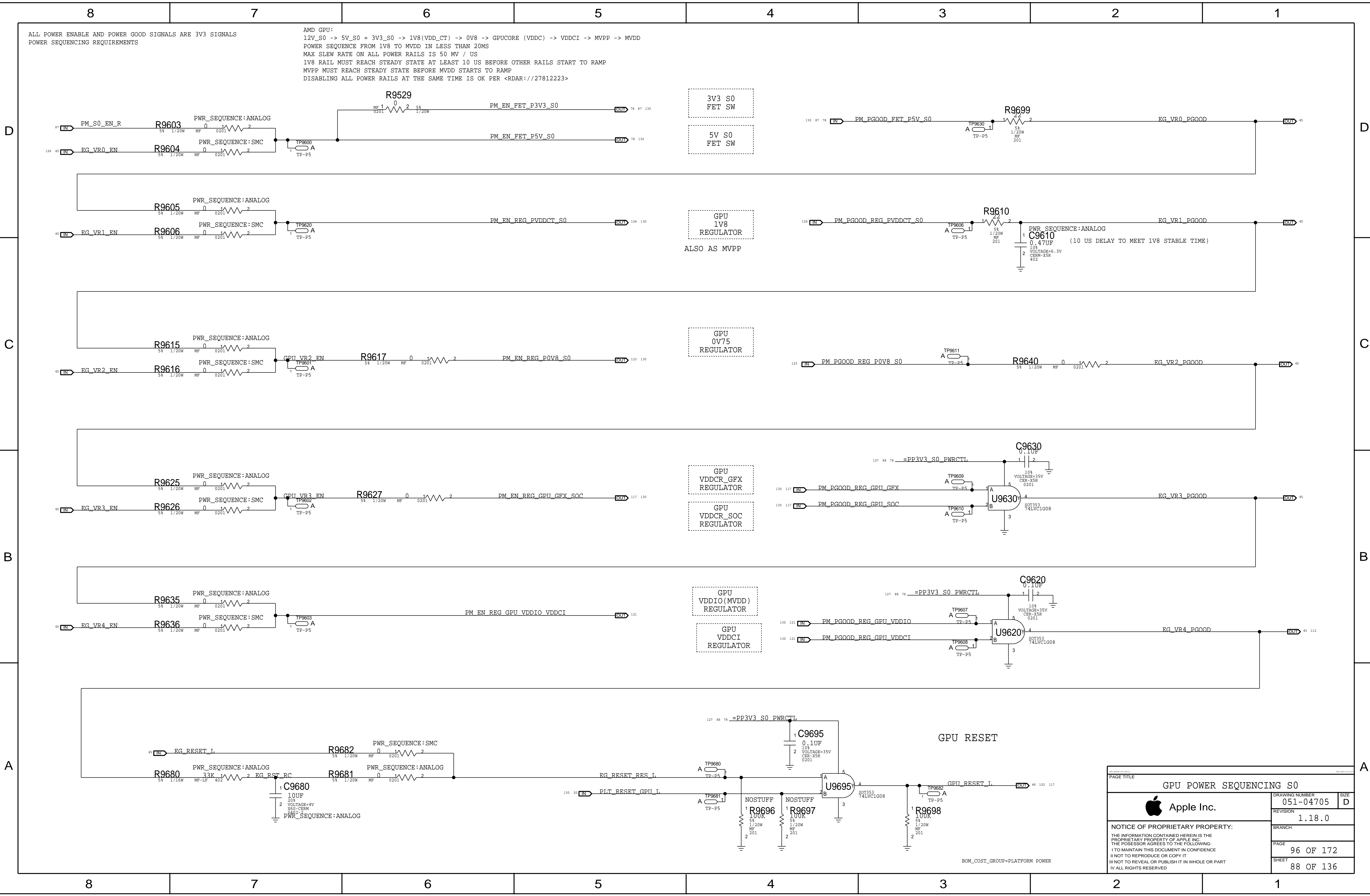
S0 CPU

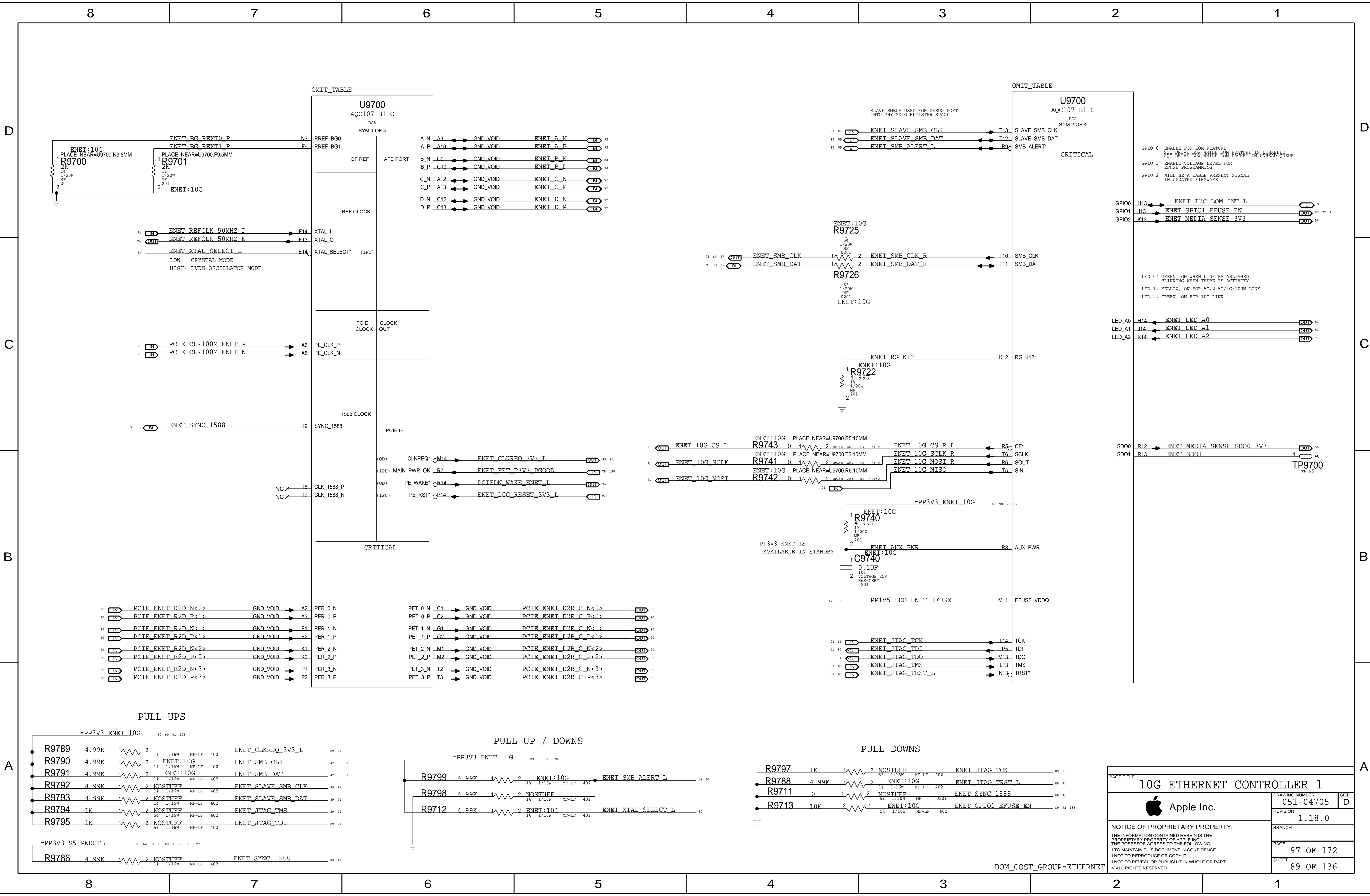
- HW + PMU sequencing



BOM_COST_GROUP=PLATFORM POWER

SYSTEM POWER SEQUENCING			
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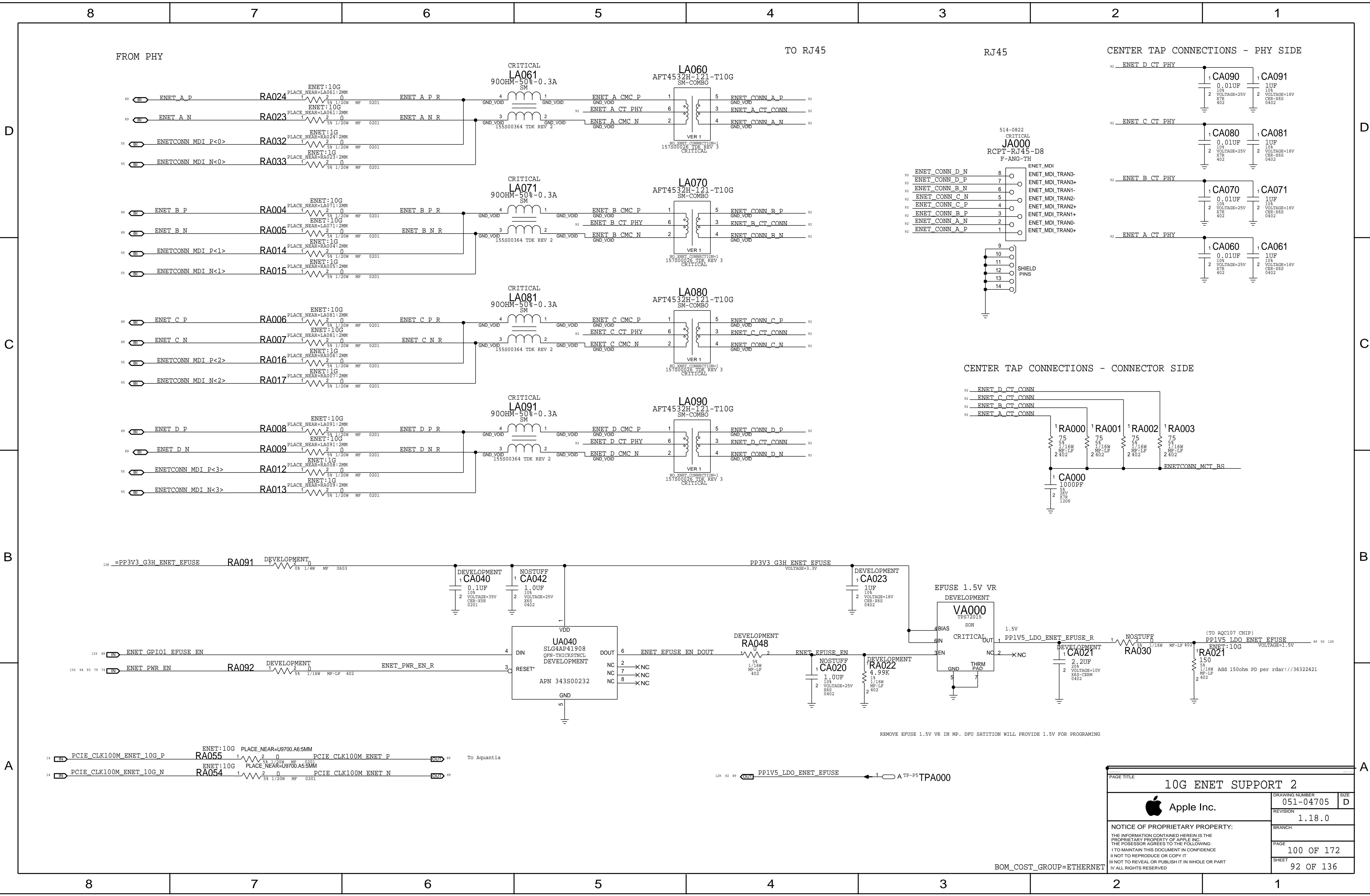
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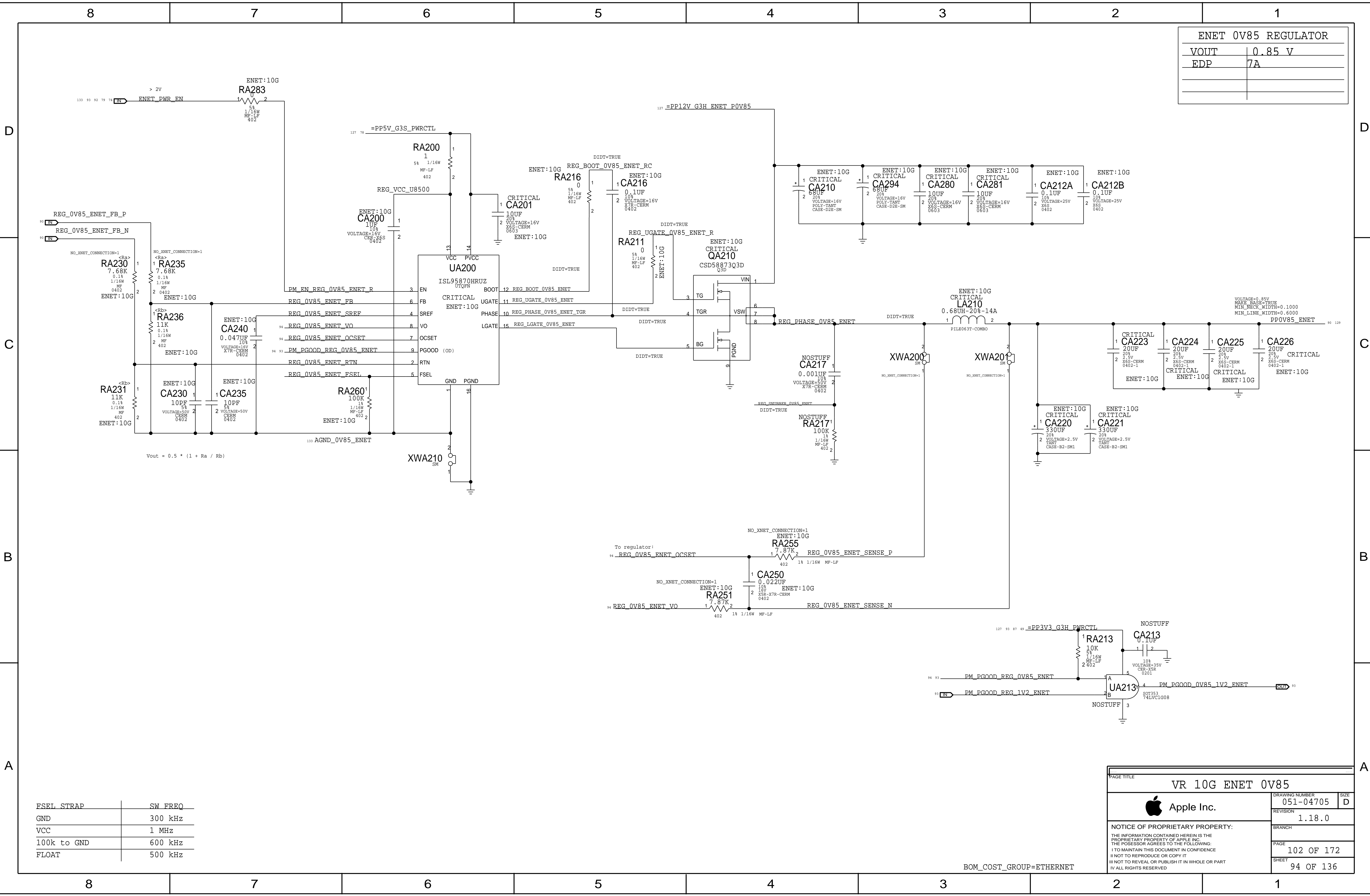
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ENET 0V85 REGULATOR	
VOUT	0.85 V
EDP	7A

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz

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VR 10G ENET 0V85		
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BOM_COST_GROUP=ETHERNET

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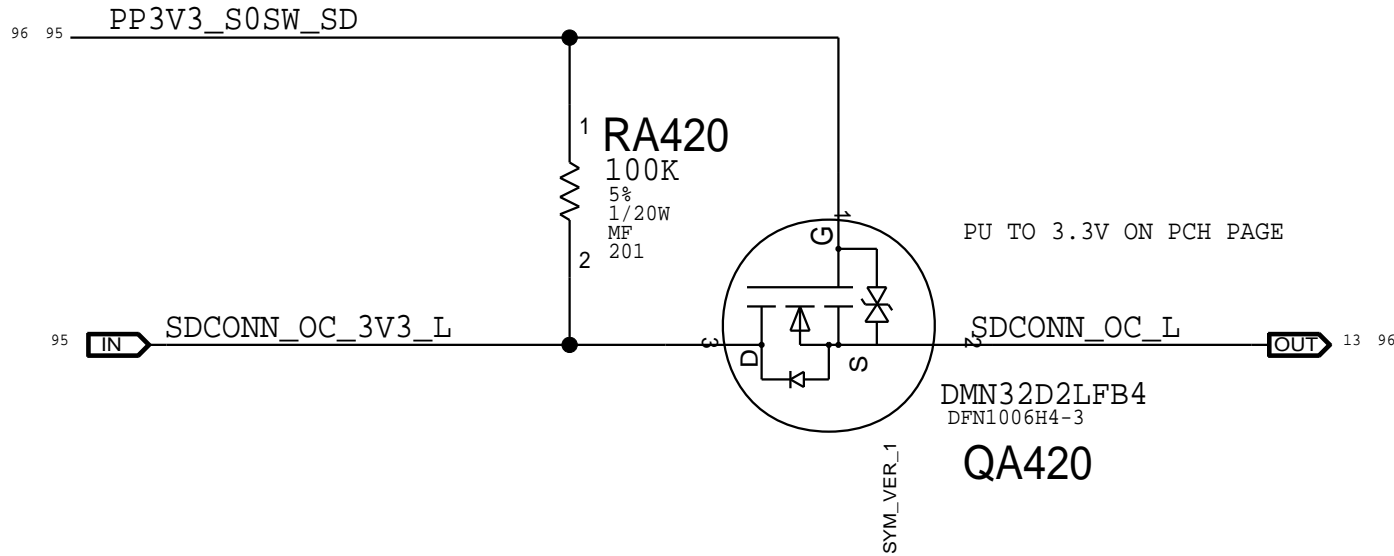
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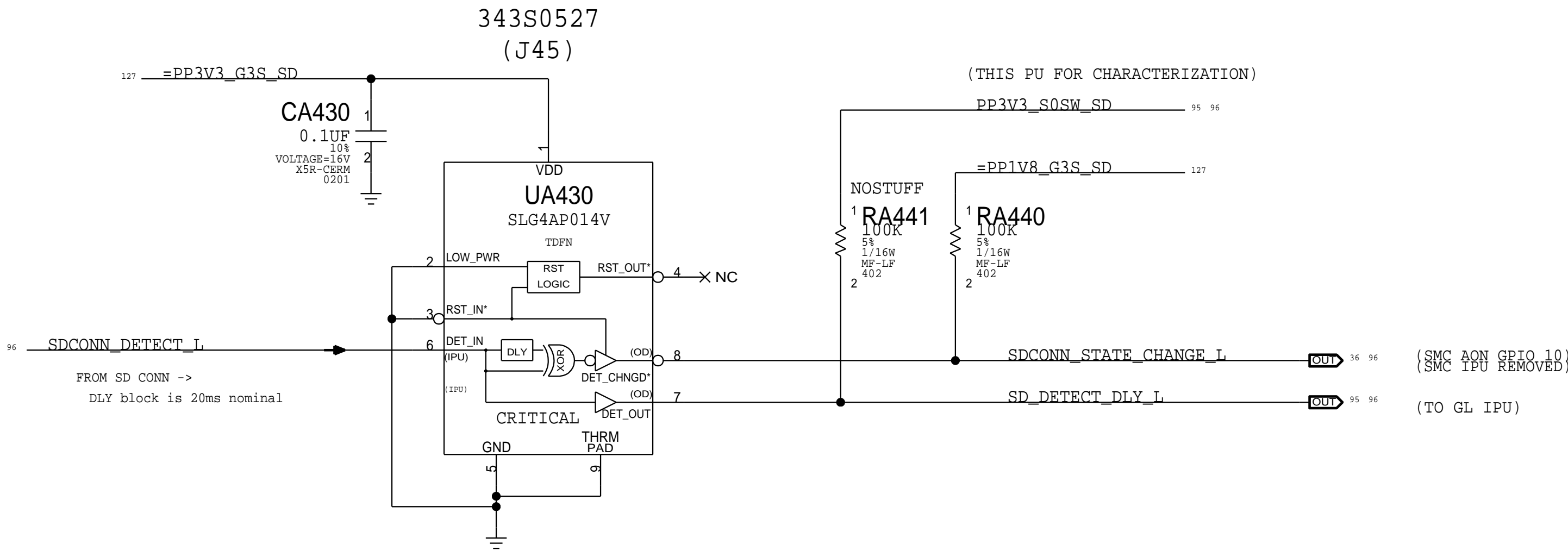
A

- TPA430A1 TP-P5 SD_SPT_CLK95
- TPA431A1 TP-P5 SD_SPT_CS_L95
- TPA432A1 TP-P5 SD_SPT_MOSI95
- TPA433A1 TP-P5 SD_SPT_MISO95
- TPA440A1 TP-P5 SDCONN_OC_L13 96
- TPA441A1 TP-P5 SDCONN_DETECT_L96
- TPA442A1 TP-P5 SDCONN_STATE_CHANGE_L36 96
- TPA443A1 TP-P5 SD_DETECT_DLY_L95 96

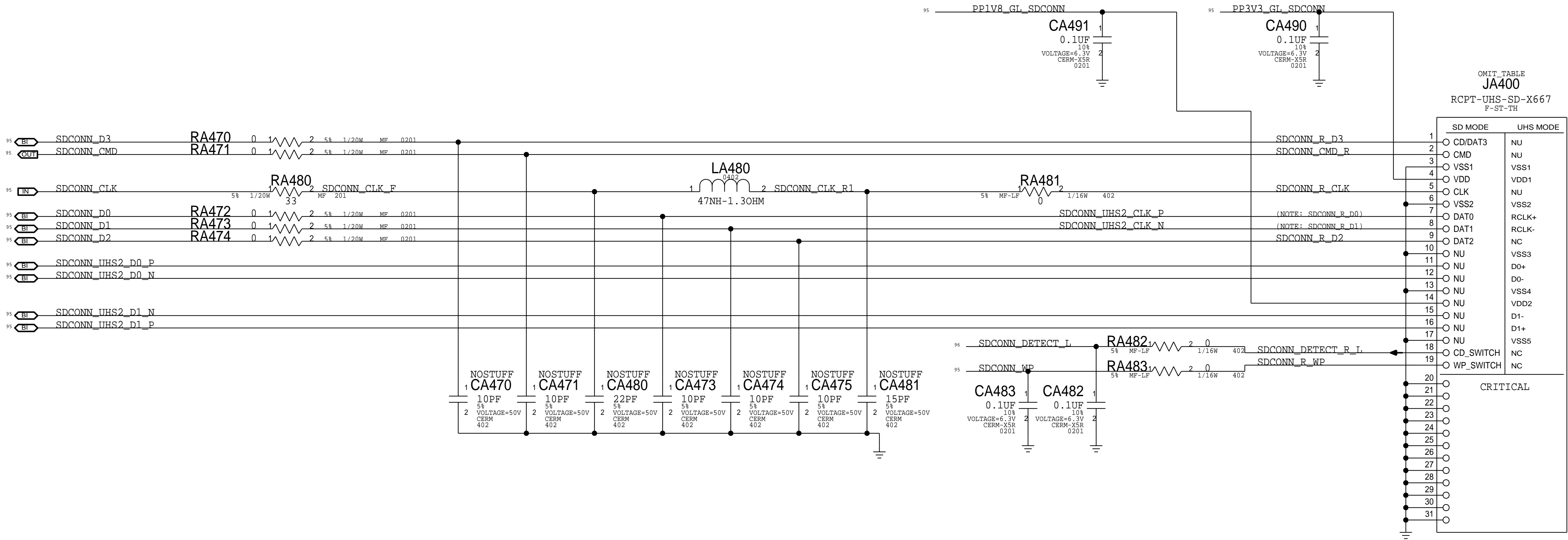
SD CARD OC EVENT ISOLATION



SDCONN STATE CHANGE AND DEBOUNCE



SD UHS-II CARD CONNECTOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
512-00005	1	CONN,RCPT,UHS SD,X1146	JA400	CRITICAL	

SD CONNECTOR UHS-II

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BOM_COST_GROUP=SD_CARD

87654321

